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(71) Applicant (*for all designated States except US*): **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): **GHYSELEN, Bruno** [FR/FR]; 58, rue Georges Maeder, F-38170 Seyssinet-Pariset (FR). **AULNETTE, Cécile** [FR/FR]; 3, Place des Tilleuls, F-38000 Grenoble (FR). **OSTERNAUD, Bénédite** [FR/FR]; 26, Rue Lieutnant Fiancey, F-38120 Saint Egreve (FR). **LE VAILLANT, Yves-Mathieu** [FR/FR]; 271, rue Gaston Angelier, F-38920 Crolles (FR). **AKATSU, Takeshi** [JP/FR]; 9, Place de l'Eglise, F-38330 Saint Nazaire Les Eymes (FR).

(74) Agents: **MARTIN, Jean-Jacques** et al.; Cabinet Regimbeau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

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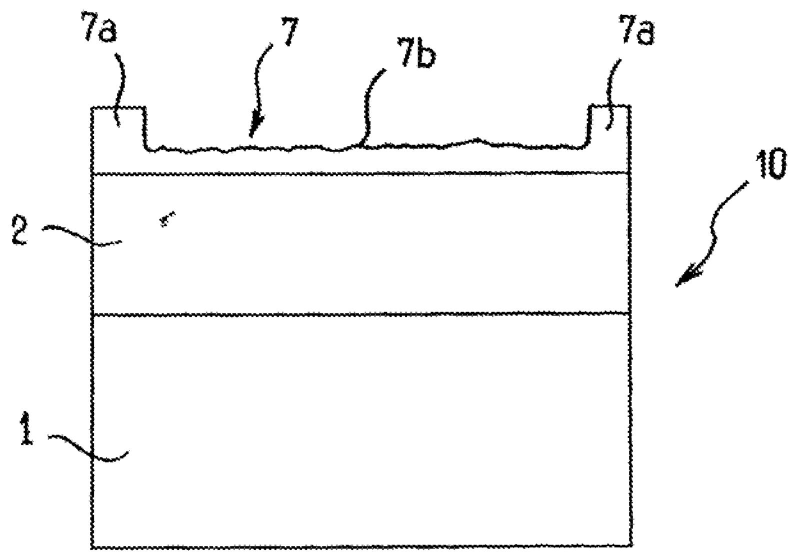
(54) Title: RECYCLING A WAFER COMPRISING A BUFFER LAYER, AFTER HAVING TAKEN OFF A THIN LAYER THEREFROM




(57) Abstract: Method of recycling a donor wafer (10) after taking off at least one useful layer, the donor wafer (10) comprising successively a substrate (1), a buffer structure (1) and, before taking-off, a useful layer. The method comprises removal of substance relating to part of the donor wafer (10) on the side where the taking-off took place, such that, after removal of substance, there remains at least part of the buffer structure (1) capable of being reused as at least part of a buffer structure (1) during a subsequent taking-off of a useful layer. The present document also relates to: - a method of producing a donor wafer (10) which can be recycled according to the invention; - methods of taking a thin layer off a donor wafer (10) which can be recycled according to the invention; - donor wafers (10) which can be recycled according to the invention.

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# "RECYCLING A WAFER COMPRISING A BUFFER LAYER, AFTER HAVING TAKEN OFF A THIN LAYER THEREFROM"

The present invention relates to the recycling of a donor wafer comprising a buffer layer after transfer of a thin semiconductor layer from the donor wafer to a receiving substrate.

The term "buffer layer" generally refers to a transition layer between a first crystalline structure such as a substrate and a second crystalline structure having the prime function of modifying properties of the material, such as structural or stoichiometric properties or atomic surface recombination properties.

In the particular case of a buffer layer, the latter may make it possible to obtain a second crystalline structure, the lattice parameter of which differs substantially from that of the substrate.

To this end, the buffer layer may have a composition which varies gradually with thickness, the gradual variation of components of the buffer layer then being directly associated with a gradual variation of its lattice parameter.

It may also have a more complex form such as a variation in composition with a variable rate, a sign inversion of the rate or discontinuous jumps in composition, possibly completed with a constant composition layer for containing defects.

Mention is then made of a metamorphic (buffer) layer or of a metamorphic embodiment, such as a metamorphic epitaxy.

Produced on the buffer layer, a layer or a superposition of layers may be taken off from the donor wafer in order to be transferred to a receiving substrate, in order to produce a particular structure.

One of the major applications of transferring thin layers formed on a buffer layer relates to the formation of strained silicon layers.

A layer is made of a material which is "strained" in tension or in compression if its lattice parameter in the interface plane is respectively greater or less than its nominal lattice parameter.

Otherwise, a layer is said to be made of a "relaxed" material if the latter is substantially close to its nominal lattice parameter, a nominal lattice parameter being the lattice parameter of the material in its bulk form in equilibrium.

When a layer is made of silicon strained in tension, some properties, such as the electron mobility of the material, are clearly improved.

Other materials, such as for example SiGe, may also be subject to a substantially similar taking-off.

The transfer of such layers onto a receiving substrate in particular by a process called Smart-cut©, and known to a person skilled in the art, then makes it possible to produce structures such as SOI (Semiconductor On Insulator) structures.

For example, after taking a layer off relaxed SiGe, the structure obtained may then act as a support for growing silicon.

Since the nominal lattice parameter of SiGe (dependent on the germanium content) is greater than the nominal lattice parameter of silicon, growth of silicon on the SGOI (Silicon-Germanium On Insulator) pseudo-substrate obtained makes it possible to provide the silicon layer strained in tension.

As an illustration, an example of such a process is described in the IBM document by L.J. Huang *et al.* ("SiGe-On-Insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors", Applied Physics Letters, 26/02/2001, vol. 78, No. 9) in which a method of producing an Si/SGOI structure is presented.

Another examples of such a process is given in the document US 2002/007481.

Other applications of metamorphic growth are possible, especially with semiconductors of the III-V family.

Thus, transistors are commonly produced using GaAs-based or InP-based technologies.

In terms of electron performance, InP has a substantial advantage over GaAs, in particular, a combination of an InP layer and an InGaAs or InAlAs layer makes it possible to improve electron mobilities.

However, the ability to market components using InP technology is limited faced with GaAs technology, particularly in terms of cost, availability, mechanical weakness and the size of bulk substrates (the maximum diameter for InP typically being 4 inches compared with 6 inches for GaAs).

A solution to this problem seems to be found with reference to a receiving

substrate, an InP layer taken off and obtained by metamorphic epitaxy of a buffer layer on a GaAs substrate.

Certain taking-off processes, such as a process of the "etch-back" type, then lead to destruction of the remaining part of the substrate and of the buffer layer during taking-off.

In some other taking-off processes, such as a Smart-cut© process, the substrate is recycled but the buffer layer is lost.

However, the metamorphic production technique is complex.

Optimizing and producing such a buffer layer may therefore involve a lengthy, difficult and expensive operation.

Furthermore, internal strains due to the variations in composition may cause the appearance of a high rate of crystalline defects, such as dislocations and point defects.

These internal strains, and therefore the generation of defects, may be minimized in particular by increasing the thickness over which the lattice parameter varies.

It is mainly for this reason that the buffer layers usually produced are thick, with a typical thickness ranging from one to a few micrometers.

However, economic and technical restraints limit some essential properties of the buffer layer, such as its thickness or a certain structural complexity.

For all these reasons among others, it would be wise to avoid completely forming a buffer layer after each recycling of the substrate.

The present invention intends to achieve this aim by providing, according to a first aspect, a method of recycling a donor wafer after having taken off at least one useful layer of a material chosen from semiconductor materials, the donor wafer comprising successively a substrate, a buffer structure and, before taking-off, a useful layer, the method comprising removal of substance on the side of the donor wafer where the taking-off took place, characterized in that, after removal of substance, at least a part of the buffer structure remains, this at least part of the buffer structure can then be reused as a buffer structure for a subsequent useful layer taking-off.

In a preferred aspects of the method of recycling according to the invention, a protective layer is further present in the donor wafer so that at least a part of the

buffer structure underlying it; the material of the protective layer being chosen from crystalline materials such that means for removing substance has an etching power which is substantially different for the material of the protective layer than for the material of at least one of the two adjacent zones, and thus is able to operate a selective removal of substance.

According to a second aspect, the invention provides a method of producing a donor wafer intended to provide a useful layer by taking-off and capable of being recycled after taking-off according to said preferred method of recycling, characterized in that it comprises the following steps:

- formation of a first part of a buffer structure on a substrate;
- formation of a protective layer on the first part of the buffer structure, in a material chosen from crystalline materials;
- formation on the protective layer of the second part of the buffer structure, such that it has a lattice parameter in the vicinity of the protective layer substantially the same as that of the first part of the buffer structure in the vicinity of the protective layer.

According to a third aspect, the invention provides a method of taking off a useful layer on a donor wafer in order to be transferred to a receiving substrate, characterized in that it comprises:

(a) bonding the donor wafer to the receiving substrate;

(b) detaching a useful layer bonded to the receiving substrate from the donor wafer,

(c) recycling the donor wafer according to said method of recycling.

According to a fourth aspect, the invention provides a method of cyclically taking off a useful layer from a donor wafer, characterized in that it comprises several steps of taking off a useful layer, each of these steps complying with the said method of taking-off.

According to a fifth aspect, the invention provides an application of the said method of cyclically taking-off or of the said method of taking-off, for producing a structure comprising the receiving substrate and the useful layer, the useful layer comprising at least one of the following materials:

SiGe, Si, an alloy belonging to the III-V family, the composition of which is respectively chosen from the possible (Al,Ga,In)-(N,P,As) combinations.

According to a sixth aspect, the invention provides donor wafers complying with the said methods according to the invention.

Other aspects, aims and advantages of the present invention will become more clearly apparent on reading the following detailed description of operating the preferred methods thereof, given by way of non-limiting example and made with reference to the appended drawings in which:

Figure 1 shows a donor wafer according to the prior art.

Figure 2 shows a donor wafer after taking-off.

Figure 3 shows a donor wafer after a first recycling step.

Figure 4 shows a first donor wafer according to the present invention.

Figure 5 shows a second donor wafer according to the present invention.

Figure 6 shows a third donor wafer according to the present invention.

Figure 7 shows the various steps of a method according to the invention successively comprising taking-off of a thin layer from a donor wafer and recycling of the donor wafer after taking-off.

The main object of the present invention consists in recycling a wafer comprising a buffer structure (i.e. any structure behaving as a buffer layer), after at least one useful layer has been taken off the wafer so as to integrate this useful layer into a semiconductor structure, the recycling including at least partial recovery of the buffer structure so that it can be reused in a subsequent taking-off.

The said recycling operation must therefore comprises a suitable treatment which does not damage at least part of the buffer structure.

Indeed, a buffer structure usually contains crystallographic defaults, such as dislocations, which can propagate and increase in size in an important manner when energy is supplied on it, this energy could provide from thermal treatments, chemical process or mechanical process.

For instance, if a buffer structure of SiGe is heated at a temperature of 350°C, 450°C or 550°C, the structural state change with respect to the temperature chosen (see for instance the document "Structural characterisation and stability of Si1-xGex/Si(100) heterostructures grown by molecular beam epitaxy" of Re et al., in the Journal of Crystal Growth, vol. 227-228, pp. 749-755, July 2001). With the increase of temperature, the buffer structure will tend to decrease its internal stress by relaxing them in slip planes, stacking defaults or other structural relaxation

types. This can bring some future difficulties at the interface with the useful layer to be formed. It is then important to keep these internal stress confined in the buffer structure.

Recycling must then carried out in a manner, with adapted means for recycling, so as to prevent and limit the extension of these crystalline stress inside the buffer structure which can damage its properties and which can thus damage the properties of the useful layer formed on it.

Advantageously, the buffer structure has a crystallographic structure which is substantially relaxed and/or without a noteworthy number of structural defects on the surface.

A "buffer layer" is as already defined more generally above in this document.

Advantageously, a buffer layer is comprised in the buffer structure and has at least one of the two following functions:

1. decreasing the density of defects in the upper layer;
2. matching a lattice parameter of two crystallographic structures with different lattice parameters.

With regard to the second function of the buffer layer, the latter is an interlayer between the two structures, and around one of its faces it has a first lattice parameter substantially identical to that of the first structure and around its other face, it has a second lattice parameter substantially identical to that of the second structure.

In the rest of this document, the buffer layers or structures described will in general comply with this latter buffer layer.

However, the present invention also relates to any buffer layer or any buffer structure as defined in this document in the most general manner.

Furthermore, an example of a method according to the invention will be described below, including recycling a donor wafer of a useful layer by taking-off, the donor wafer initially consisting of a support substrate and a buffer structure.

With reference to Figure 1, a donor wafer 10 (donor of a thin layer by taking-off) included in the known prior art consists of a support substrate 1 and a buffer structure I.

The application for this donor wafer 10 in the present invention is that of taking off a useful layer, from the part 4 of the buffer structure I and/or at least part of an overlayer formed on the surface of the buffer structure I (not shown in Figure 1), in order to integrate it into a structure, such as an SOI structure.

The support substrate 1 of the donor wafer 10 comprises at least one semiconductor layer having a first lattice parameter at its interface with the buffer structure I.

In a particular configuration, the support substrate 1 consists of a single semiconductor having the first lattice parameter.

In a first configuration of the buffer structure I, the latter consists of a buffer layer 2.

The buffer layer 2, located on the support substrate 1, in this case makes it possible to present at its surface a second lattice parameter substantially different from the first lattice parameter of the substrate 1, and thus to have, in the same donor wafer 10, two layers 1 and 4 respectively having different lattice parameters.

Furthermore, the buffer layer 2 may make it possible, in some applications, for the overlying layer to prevent the latter from containing a high defect density and/or being subject to noticeable stresses.

Furthermore, the buffer layer 2 may make it possible, in some applications, for the overlying layer to have a good surface condition.

In general, the buffer layer 2 has a lattice parameter which changes gradually with thickness in order to establish the transition between the two lattice parameters.

Such a layer is generally called a metamorphic layer.

This gradual change of the lattice parameter may be produced continuously within the thickness of the buffer layer 2.

Alternatively, it may be carried out in "stages", each stage being a thin layer with a substantially constant lattice parameter which is different to that of the underlying stage, so as to discretely change the lattice parameter stage by stage.

It may have also have a more complex form, such as a variation in composition with a variable rate, a sign inversion of the rate or discontinuous jumps in composition.

The change of the lattice parameter in the buffer layer 2 is advantageously

found by increasing therein, starting from the substrate 1, in a gradual manner, the concentration of at least one atomic element which is not contained in the substrate 1.

Thus, for example, a buffer layer 2 produced on a substrate 1 made of a unitary material could be made of a binary, tertiary, quaternary or higher material.

Thus, for example, a buffer layer 2 produced on a substrate 1 made of a binary material could be made of a tertiary, quaternary or higher material.

The buffer layer 2 is advantageously produced by growth on the support substrate 1, for example by epitaxy, using known techniques such as the CVD and MBE techniques (abbreviations for "Chemical Vapour Deposition" and "Molecular Beam Epitaxy", respectively).

In general, the buffer layer 2 may be produced by any other known method, in order to obtain, for example, a buffer layer 2 consisting of an alloy of various atomic elements.

A minor step of finishing the surface of the substrate 1 underlying the buffer layer 2, for example by CMP polishing, may possibly precede the production of the buffer layer 2.

In a second configuration of the buffer structure I, and with reference to Figure 1, the buffer structure I consists of a buffer layer 2 (substantially identical to that of the first configuration) and of an additional layer 4.

The additional layer 4 may be between the substrate 1 and the buffer layer 1, or on the buffer layer 1, as shown in Figure 1.

In a first particular case, this additional layer 4 may constitute a second buffer layer, such as a buffer layer making it possible to confine defects, and thus to improve the crystalline quality of a layer produced on the buffer structure I.

This additional layer 4 is made of a semiconductor preferably having a constant material composition.

The choice of the composition and of the thickness of such a buffer layer 4 to be produced are then particularly important criteria to achieve this property.

Thus, for example, the structural defects in an epitaxially grown layer usually decrease gradually within the thickness of this layer.

In a second particular case, the additional layer 4 is located on the buffer layer 1 and functions as an upper layer to the buffer layer 2.

Thus it may fix the second lattice parameter.

In a third particular case, the additional layer 4 is located on the buffer layer 1 and plays a role in the taking-off that will be carried out in the donor wafer 10, such as a taking-off at its level.

The additional layer may also have several functions, such as functions chosen from these last three particular cases.

In an advantageous configuration, the additional layer 4 is located on the buffer layer 2 and has a second lattice parameter different from the first lattice parameter of the support substrate 1.

In a particular case of this latter configuration, the additional layer 4 is made of a material relaxed by the buffer layer 2, and has the second lattice parameter.

The additional layer 4 is advantageously produced by growth on the buffer layer 2, for example by epitaxial growth by CVD or MBE.

In a first embodiment, the growth of the additional layer 4 is carried out *in situ*, directly in continuation with the formation of the underlying buffer layer 2, the latter also in this case being advantageously formed by layer growth.

In a second embodiment, the growth of the additional layer 4 is carried out after a minor step of finishing the surface of the underlying buffer layer 2, for example by CMP polishing, heat treatment or other smoothing techniques such that the dislocations and other defaults contained in the buffer layer 2 don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the final buffer structure I thus formed.

The taking-off of a useful layer from the donor wafer 10 is operated according to one of the following main modes:

(1) the useful layer to be taken off is part of the additional layer 4.

(2) the useful layer to be taken off is part of an overlayer (not shown in Figure 1) which has been formed beforehand on the buffer structure I, for example by epitaxial growth possibly preceded by finishing the surface of the buffer structure I.

The donor wafer 10 then functions as a substrate for the growth of the overlayer.

The latter may comprise one or more thin layers depending on the taking-off

mode that it is desired to use.

Furthermore, advantageously, it has a lattice parameter substantially identical to that of the relaxed material of the free face of the buffer structure I, such as a layer of an identical material, or another material which would have all or some of its crystallographic structure strained in tension or in compression, or the combination of these two types of material.

In a particular embodiment of the donor wafer 10, one or more interlayers are furthermore inserted between the buffer structure I and the overlayer. In this case, this or these interlayers are not removed.

(3) The useful layer to be taken off is part of the additional layer 4 and an overlayer (formed in a substantially identical manner to that described in the second taking-off mode).

Whatever the taking-off mode chosen, and with reference to Figure 2, after taking-off and in the majority of cases, projecting parts 7a and/or rough parts 7b appear on the taking-off surface of the remaining donor wafer 10.

This taking-off surface "in relief" belongs to a post-taking-off layer 7 located above the buffer layer 2.

This post-taking-off layer 7 consists of all or some of the layer 4, possibly one or more interlayers and possibly part of an overlayer depending on the taking-off mode chosen from the three previously discussed taking-off modes.

The parts 7a and 7b in relief appearing on the surface of the post-taking-off layer 7 mainly depend on the taking-off mode and on the technique operated during taking-off.

- Thus, for example, a taking-off mode currently used in industry consists in taking off the useful layer not over the entire surface of the donor wafer 10, but only over part of the latter (which is generally a substantially centred part) leaving, on the surface of the donor wafer 10, projecting parts, such as those referenced 7a. These projecting parts are generally integral and located at the periphery of the surface of the donor wafer 10, all the projecting parts then being known in the business as "taking-off ring".

- Thus, for example, known taking-off techniques such as, for example, those that we will study further and later on in this document, such as the Smart-cut© technique already mentioned, sometimes cause surface roughness

such as that referenced 7b on the taking-off surface.

Once the taking-off is carried out, recycling according to the invention is operated in order to restore the donor wafer 10.

Generally, recycling comprises two steps:

- removing substance;
- restoring at least part of the donor wafer 10.

The first step of recycling according to the present invention consists in removing at least the relief parts 7a and 7b (shown in Figure 2).

This removal of substance according to the invention is operated such that, after the removal, at least part of the buffer structure I remains, which can be used again during subsequent taking-off of a new useful layer.

The remaining part of the buffer structure I, after removal of substance, is thus recycled, unlike the known recycling of the prior art.

In a first particular case of recycling, and concerning the said second mode of taking-off (2), it could be advantageous to choose a thickness of the overlayer so that, after taking-off, the remaining part of the overlayer (which is the post-taking-off layer 7) is removed by standard mechanical means for removing substance, such as polishing means or CMP, without removing substance from the safe buffer structure I, and thus preserve the entire buffer structure I.

Thickness of material removed during the recycling by standard mechanical means like polishing is typically of around 2 micrometers, even if current development succeeds to reach thickness around 1 micrometer.

In a second particular case of recycling, and concerning the said second mode of taking-off (2), it could be advantageous to chose a thickness of the overlayer and of the additional layer 4 so that, after taking-off, the remaining part of the overlayer (which is the post-taking-off layer 7) and at least a part of the additional layer 4 is removed by standard mechanical means for removing substance, such as polishing means or CMP, without removing substance from the safe buffer layer 2, and thus preserve the entire buffer layer 2.For another particular case of recycling, the removal of substance advantageously comprises using of means for chemically attacking materials, such as chemical etching.

The etching may be solely chemical, electrochemical, photo-electrochemical, or any other equivalent etching, such as the etching used during

chemical-mechanical polishing.

In an advantageous etching mode, selective etching is carried out.

Thus, in particular, it is possible to use an etching fluid (that is to say a gas or a solution) suitable for carrying out selective etching of a material to be removed from a material to be recycled, the two materials belonging to adjacent layers, so that the material to be recycled forms an etch-stop layer, thus efficiently taking off the part to be removed while protecting the layer to be recycled from the chemical etching.

The property of selectivity between the two materials may, for example, be obtained in at least one of the following cases:

- the two materials are different; or

- the two materials contain atomic elements which are substantially identical except for at least one atomic element; or

- the two materials are substantially identical, but at least one atomic element in one material has an atomic concentration which is substantially different from that of the same atomic element in the other material; or

- the two materials have different porosity densities.

It is known, for example, that SiGe behaves as a stop layer when etching Si with a solution containing compounds such as KOH (potassium hydroxide, selectivity of about 1:100), $NH_4OH$ (ammonium hydroxide, selectivity of about 1:100) or TMAH (tetramethyl ammonium hydroxide).

It is known, for example, that when SiGe has a germanium concentration greater than or equal to 25%, it behaves as a stop layer when etching SiGe having a germanium concentration less than or equal to 20%, with a solution containing compounds such as TMAH.

It is known, for example, that if Si is suitably doped with a doping element at a selected concentration, such as boron at more than $2 \times 10^{19}$ $cm^{-3}$, it behaves as a stop layer when etching an undoped Si material with a solution containing compounds such as EDP (ethylenediamine pyrocatechol), KOH or $N_2H_2$ (hydrazine).

It is known, for example, that porous Si is etched by selective etching with respect to non-porous crystalline Si, with a solution containing compounds such as KOH or $HF + H_2O_2$.

Thus it is possible to selectively etch the additional layer 4 with respect to the buffer layer 2, and/or the possible overlayer with respect to the additional layer 4 or the possible interlayer.

This removal of substance by chemical means may also be accompanied by using mechanical means for attacking substance or other means.

In particular, it is possible to carry out CMP polishing with a selective chemical etching solution.

This chemical etching may also be preceded or followed by a removal of substance operated by mechanical means of eroding substance such as polishing, grinding, attack or by any other means.

In general, the removal of substance may comprise using any other means of attacking substance capable of removing substance without completely taking off and damaging at least part of the buffer structure I.

One of the following substance removal modes is therefore used:

(a) removing part of the post-taking-off layer 7 comprising at least the relief parts 7a and 7b; or

(b) removing the entire post-taking-off layer 7; or

(c) removing the entire post-taking-off layer 7 and part of the buffer layer 2.

If the post-taking-off layer 7 comprises part of an original overlayer, the substance removal mode (a) then preferably comprises completely taking off this overlayer part.

With reference to Figure 3, the part of the original buffer structure which remains after substance removal is referenced I'.

It consists of:

- the entire original buffer structure I when the substance removal mode (a) was used and when the latter did not involve taking off any part of the additional layer 4; or

- the buffer layer 2 and part of the additional layer 4 when the substance removal mode (a) was used and when the latter involved taking off part of the additional layer 4; or

- the buffer layer 2 when the substance removal mode (b) was used; or

- part of the buffer layer 2 when the substance removal mode (c) was used.

The second recycling step comprises, after the first recycling step relating to substance removal, reforming at least some of the layers taken off during the first step.

First of all, and in certain cases, it will be preferred to finish the surface of the donor wafer 10 where the substance removal operated during the first recycling step took place, so as to take off any roughness which may have appeared during the substance removal.

To this end, for example CMP polishing, a heat treatment or another smoothing technique will be used such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

This second recycling step involves restoring the buffer structure I from the remaining buffer structure I', when part of the original buffer structure I was removed during the first recycling step.

Advantageously, the restoration of the buffer structure I is such that, once formed, the latter is substantially identical to the original buffer structure I.

However, in a particular embodiment, it will be possible to slightly alter some production parameters in order to obtain a buffer structure I which is slightly different from the original. For example, the concentrations of certain compounds in a material will be slightly altered.

Restoring the buffer structure I involves reforming the removed part of the buffer layer 2 when part of the original buffer layer 2 was cut away during the first recycling step.

Restoring the buffer structure I involves reforming all or part of the additional layer 4 when all or part of the original additional layer 4 was cut away during the first recycling step.

In this case, it will be possible to produce an additional layer 4 with a thickness substantially identical to or substantially different from the original.

Once the buffer structure I is restored, an overlayer may possibly be formed above it, which overlayer will at least partly comprise a new useful layer to be taken off, possibly with one or more interlayers between the buffer structure I and the overlayer.

The layers possibly formed during this second recycling step are advantageously produced by layer growth on their respective underlying layers, for example by CVD or MBE epitaxial growth.

In a first case, at least one of these layers is grown *in situ*, directly in continuation with the formation of the underlying growth support, the latter also being formed in this case advantageously by layer growth.

In a second case, at least one of these layers is grown after a minor step of finishing the surface of the underlying growth support, for example by CMP polishing, heat treatment or other smoothing techniques, such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

Thus, a donor wafer 10 which is substantially identical to the original, that is to say the donor wafer 10 shown in Figure 1, is finally obtained, with the exception of modifications desired and carried out by a person skilled in the art.

The donor wafer 10 obtained in this way comprises at least part of the original buffer structure I, and therefore at least part of the original buffer layer 2, which makes it possible to avoid its complete, lengthy and expensive reformation, as was the case in the known recycling methods.

Donor wafers 10, which can be recycled according to the particular operational modes of the recycling methods presented above, are described in the rest of the document, they provide particularly effective protection for at least part of the buffer structure I during matched recycling.

The donor wafers 10, which are shown in Figures 4, 5 and 6, each involve a substrate 1 and a buffer structure I, like the donor wafer 10 shown in Figure 1.

Each of these donor wafers 10 further comprises a protective layer 3 located in the part located on the same side of the buffer structure I as the interface of the latter with the substrate 1.

A protective layer 3, as defined in the present invention, is made of a material chosen from crystalline materials, such as semiconductors, so as to have the prime function of protecting that part of the donor wafer 10 which is subjacent to it, and which comprises at least part of the buffer structure I, during at least one of the substance removing treatments used during the recycling.

Advantageously, the protective layer 3 is produced by layer growth on the underlying growth support, for example by CVD or MBE epitaxial growth.

In this configuration, and in a first case, the growth of the protective layer 3 is carried out *in situ*, directly in continuation with the formation of the layer which is subjacent to it, the latter also in this case being advantageously formed by layer growth.

In a second case, the growth of the protective layer 3 is carried out after a minor step of finishing the surface of the layer which is subjacent to it, for example by CMP polishing, heat treatment or other smoothing techniques, such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

The material of the protective layer 3 is chosen such that there is at least one means for removing substance having an ability to attack the material forming the protective layer 3 which is substantially different from the material of at least one of the two zones adjacent to the protective layer 3.

And is thus capable of operating a selective substance removal.

The selective substance removal operated at the protective layer 3 is at least one of the following selective substance removal modes:

- selective removal of the material in the zone adjacent to the protective layer 3 and located on the side of the useful layer which has been taken off, with respect to the protective layer 3, the protective layer 3 forming a stop layer for substance removal;

- selective removal of the material of the protective layer 3, the zone adjacent to the protective layer 3 and located on the side of the substrate 1 as the protective layer 3 forming a layer stopping substance removal.

It is also possible, in one particular operation of selective substance removal, to combine the successive operation of two selective substance removal modes for the same protective layer 3.

Thus, the layer above the protective layer 3, then the protective layer 3 are selectively removed.

Whatever the selective substance removal mode chosen for operation during the first recycling step, and intended to remove that part of the donor wafer 10

located on the side of the taken off useful layer, there is a layer stopping substance removal (the protective layer 3 in the case of the first selective substance removal or the zone adjacent to the protective layer 3 located on the same side of the substrate 1 as the protective layer 3 in the case of the second selective substance removal).

Thus, the stop layer acts as a barrier to the attack of substance, and in the same way, protects the material of the part underlying the protective layer 3 (which comprises at least part of the buffer structure I).

In some cases, it will be desired that the protective layer 3 does not substantially disturb the crystallographic structure of the adjacent layers, and in particular, that it does not disturb the crystalline growth of the underlying layer to be formed, the lattice parameter of which must, in most cases, substantially comply with the lattice parameter of the part underlying the protective layer 3.

This last point is particularly important when the protective layer 3 is located in the buffer structure I (shown in Figure 4).

This result is achieved according to several embodiments of the protective layer 3, as explained below:

In a first embodiment of the protective layer 3, the protective layer 3 is restricted to having its lattice parameter substantially identical to that of the zones which are adjacent to it, even if the nominal lattice parameters of these two materials are substantially different from that of the protective layer 3.

Two main conditions must therefore be met for this operation to succeed:

- the respective nominal parameters of the protective layer 3 and of the zone underlying it do not have values which are too different from each other, so as to avoid the appearance of defects (such as dislocations or local strains) in the protective layer 3;
- the protective layer 3 must be sufficiently thin to prevent progressive relaxation of the strain in the thickness of the layer and/or generation of defects. For this, the thickness of such a protective semiconductor layer 3, made of a strained crystalline material, must be less than a critical thickness known to a person skilled in the art, and especially depending on the materials forming it, the materials of the layers which are adjacent to it, and techniques for producing the strained layer. Critical thicknesses typically encountered are

thus less than or equal to several hundred angstroms.

Some examples of "standard critical thickness" can be found in "High-Mobility Si and Ge structures" of Friedrich Schaffler ("Semiconductor Science Technology" 12 (1997) 1515-1549).

In a second embodiment of the protective layer 3, a material is chosen for the protective layer 3 which has a nominal lattice parameter substantially close to that of the materials forming the zones which are adjacent to it.

Thus, unlike the first embodiment, the crystallographic structure of the protective layer 3 is relaxed in this case.

To this end, and also in order to satisfy a criterion of selectivity during substance removal operated during the first recycling step, a material will, for example, be chosen for the protective layer 3, at least one constituent element of which is different from those of the materials which are adjacent thereto, while keeping a lattice parameter close to that of the adjacent zones, this constituent element is thus the main element which will determine the selectivity with respect to the adjacent layer in question.

In a particular case, no constituent element of the material of the protective layer 3 is found in the material constituting the adjacent zone involved in the selective substance removal, the two materials are thus completely different.

In another particular case, each different constituent element of the protective layer 3 with respect to the adjacent zone involved in the selective removal of substance may be an additional element or an element missing from the adjacent layer in question.

For example, it will be possible to dope a protective layer 3 having substantially the same lattice parameter as that of the adjacent zones so as not to substantially disturb this lattice parameter after doping.

If the protective layer 3 consists of the same material as that of the zone which is adjacent thereto and involved in the selective substance removal, this doping element is the element which will then determine the selectivity ability.

In the case of doping the protective layer 3, the thickness of the protective layer 3 must however, in some cases, remain less than a certain critical thickness, known to a person skilled in the art, if it is desired that defects, such as dislocations, in particular of the screw type, are not to appear.

In a third embodiment of the protective layer 3, the surface of a previously produced layer is made porous in order to form a porous layer.

This porosification may be carried out by anodization, by implantation of atomic species, or by any other porosification technique, as described, for example, in document EP 0 849 788 A2.

This layer of porous material may produce, when at least one adjacent material may undergo a selective substance attack determined by a suitable attack means, a protective layer 3.

This protective layer 3 is preferably between two adjacent layers, that is to say between the layer whose surface has been porosified and a layer formed on the layer of porous material, having substantially identical respective materials.

Since the porosity does not substantially disturb the crystallographic structure of these two adjacent layers, such a protective layer 3 therefore does not substantially disturb the crystallographic structure of the donor wafer 10.

Thus, a crystallographic structure is obtained for the protective layer 3 which is very close or even substantially identical to that of the zones which are adjacent thereto, the protective layer 3 therefore not disturbing the crystallography of the surrounding structure.

However, in other cases, it will be possible to have a protective layer 3 having some influence on the lattice parameter of the surrounding structures, the complete or relative strain or relaxation state that the protective layer 3 is then capable of causing to the adjacent layers shows, in these particular cases, a property considered as being of minimum benefit for the downstream application.

Several selective substance removal techniques may be operated at the protective layer 3.

A first selective substance removal technique consists in applying friction forces to the protective layer 3 in order to take off at least part of the substance to be removed.

These friction forces may, for example, be applied by a polishing plate, possibly combined with abrasive action and/or chemical action.

The material which forms the protective layer 3 is chosen from crystalline material so that there is a mechanical substance attack method having a mechanical attack power which is substantially different for the material forming the protective

layer 3 than for the material of at least one of the two zones adjacent to the protective layer 3, and thus being capable of operating at least one selective mechanical attack method.

The selective mechanical attack method is therefore one of the following mechanical attack methods:

- selective mechanical attack of the material of the zone adjacent to the protective layer 3 and located on the side as the useful layer which has been taken off, with respect to the protective layer 3.

The material of the protective layer 3 thus has properties of withstanding mechanical attack which are substantially greater than in the region which lies over it.

For this purpose, it is possible for example to harden the protective layer 3 with respect to the overlying layer, in a manner suitable for the mechanical attack method chosen to remove the overlying zone.

Thus, for example, it is known that carbonated Si, with a typical C concentration of between 5% and 50%, is harder than uncarbonated Si.

- Selective mechanical attack of the material of the protective layer 3, the zone adjacent to the protective layer 3 and located on the same side of the substrate 1 with regard to the protective layer 3 forming an etch-stop layer.

The material of the protective layer 3 has properties of withstanding mechanical attack, and especially erosion, which are substantially less than in the zone which lies over it.

For example, it is possible to soften the protective layer 3 with respect to the underlying layer, in a manner suitable for the substance removal technique chosen to remove the protective layer 3.

A second selective substance removal technique consists in chemically etching the substance to be removed.

Wet etching may be operated with etching solutions suitable for the materials to be removed.

Dry etching may also be operated in order to remove substance, such as plasma etching or sputtering.

Furthermore, the etching may be solely chemical, electrochemical or

photo-electrochemical.

The material which forms the protective layer 3 is chosen from the crystalline materials so that there is an etching fluid (a gas or a solution) having an ability to etch the material forming the protective layer 3 which is substantially different from the material of at least one of the two zones adjacent to the protective layer 3, and thus being capable of carrying out at least one selective etching method.

The selective etching method is one of the following etching methods:

- selective etching of the material of the zone adjacent to the protective layer 3 and located on the side of the useful layer which has been taken off, with respect to the protective layer 3, the protective layer 3 forming an etch-stop layer;

- selective etching of the material of the protective layer 3, the zone adjacent to the protective layer 3 and located on the same side of the substrate 1 with respect to the protective layer 3 forming an etch-stop layer.

Whatever the selective etching method likely to be operated during the recycling and intended to remove that part of the donor wafer 10 located on the same side of the taken off useful layer, there is an etch-stop layer (the protective layer 3 in the case of the first etching method or the zone adjacent to the protective layer 3 located on the same side of the substrate 1 as the protective layer 3 in the case of the second selective etching method).

Thus, the stop layer acts as a barrier to chemical etching, and in the same way protects the material of the part underlying the protective layer 3 (which comprises at least part of the buffer structure I).

As has already been stated above, the selectivity for removing substance between the material of the protective layer 3 and the material of the adjacent zone involved in the selective etching may be obtained by the fact that:

- the two materials are different; or

- the two materials contain substantially identical atomic elements, except for at least one atomic element; or

- the two materials are substantially identical, but at least one atomic element in one material has an atomic concentration which is substantially different from that of the same atomic element in the other material; or

- the two materials have different porosity densities.

With reference to Figure 4, the protective layer 3 is within the buffer structure I, the donor wafer 10 thus comprises a structure consisting of the following four successive layers: the support substrate 1, a lower part 2' of the buffer structure I, the protective layer 3 and the upper part 4' of the buffer structure I.

Here, the protective layer 3 makes it possible to protect the lower part 2' of the buffer structure I.

Recycling such a donor wafer 10 according to the invention consists, during a first step, in taking off all of the part located on the same side of the upper part 4' of the buffer structure I as the protective layer 3.

At the protective layer 3, the selective substance removal mode is at least one of the following selective substance removal modes:

- removal of the material from the zone of the part 4' adjacent to the protective layer 3, the protective layer 3 forming a layer stopping the removal of substance;

- removal of material from the protective layer 3, the zone of the part 2' adjacent to the protective layer 3 forming a layer stopping the removal of substance.

Whatever the selective substance removal mode likely to be operated during the recycling and intended to remove the part 4' adjacent to the protective layer 3, there is a layer stopping the removal of substance (the protective layer 3 in the case of the first selective substance removal mode or the zone of the part 2' adjacent to the protective layer 3, in the case of the second selective substance removal mode), thus acting as a barrier to substance attack or etching, and in the same way protecting the material of the lower part 2' of the buffer structure I.

So that the crystallographic structure of the buffer structure I is not substantially disturbed, this type of protective layer 3 must have its own crystallographic structure which is substantially identical to that of the zone adjacent to the buffer structure I, and must therefore be produced according to an embodiment which makes it possible to obtain this material property, such as one of the three embodiments already discussed.

After the said removal of the substance lying over the lower part 2' of the buffer structure I, the recycling advantageously comprises production of a new

upper part 4' of the buffer structure I, and possibly of a new protective layer 3 where the latter has been removed (during the second selective substance removal mode mentioned above or by a treatment suitable for removing this layer 3).

These layers 3 and 4' may be grown *in situ* or after a minor step of finishing the surface of the donor wafer 10 on which the growth(s) will take place, for example by CMP polishing, heat treatment or other smoothing techniques, such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

The lower part 2' of the buffer structure I is therefore preserved during recycling, which is not the case with the methods of the prior art.

In a particular and advantageous configuration of the donor wafer 10, the lower part 2' of the buffer structure I is a buffer layer, and the upper part 4' of the buffer structure I is an additional layer to the buffer layer, such as the buffer layer 2 and additional layer 4 shown in Figure 1 and discussed above.

This particular configuration has the advantage of protecting the buffer layer 2', that is to say, that part of the buffer structure I which is generally the most difficult, the longest and the most expensive to produce.

Since the additional layer 4' is usually formed by epitaxial growth, combined with fixed parameters (such as for example the concentration of the elements to be epitaxially grown, the temperature, the pressure, the atmosphere, the growth speed and rate, etc.), and is itself the subject of taking-off during the step of taking off the layer from the donor wafer 10, protecting this additional layer 4' by the protective layer 3 during recycling does not seem necessary.

However, in another particular configuration of the donor wafer 10, the protective layer 3 can be located within the additional layer 4' in order to protect at least part thereof.

And in another particular configuration, the protective layer 3 is formed inside the buffer layer 2' in order to protect only part thereof, for example the part which is most difficult to produce.

With reference to Figure 5, a second donor wafer 10 according to the invention differs mainly from the donor wafer 10 shown in Figure 2 in that the protective layer 3 is no longer located in the buffer structure I, but directly over the

buffer structure I.

Furthermore, an overlayer 5 is present on the protective layer 3, in which at least part of a useful layer will be taken off on transfer of a layer from the donor wafer 10.

The composition and the crystallographic structure of this overlayer 5 will be chosen depending on the physical, electrical and/or mechanical properties that it is desired to obtain in the post-transfer structure.

The material of this overlayer 5 may, for example, have a nominal lattice parameter substantially identical to that of the buffer structure I in its part adjacent to the protective layer 3, so as to preserve a substantially relaxed structure.

The material of this overlayer 5 may also have, for example, a nominal lattice parameter substantially different from that of the buffer structure I in its part adjacent to the protective layer 3, and have a thickness which is sufficiently small so that it has to preserve the lattice parameter of the buffer structure I in its part adjacent to the protective layer 3, and thus be strained.

The material of this overlayer 5 may again be chosen, for example, in order to have a structure intermediate between a strained structure and a relaxed structure.

In an advantageous configuration, the overlayer 5 is produced by layer growth, for example by CVD or MBE epitaxial growth.

In this configuration, and in a first case, the growth of the overlayer 5 is carried out *in situ*, directly in continuation with the formation of the upper part of the buffer structure I, the latter in this case also being advantageously formed by layer growth.

In a second case, the growth of the overlayer 5 is carried out after a minor step of finishing the surface of the upper surface of the underlying buffer structure I, for example by CMP polishing, heat treatment or other smoothing techniques, such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

With regard to the protective layer 3, its role in this case is to protect substantially all of the underlying buffer structure I and the substrate 1 from the substance removal operated during the first recycling step.

The recycling of such a donor wafer 10, after a useful layer has been taken off from it in the overlayer 5, consists, during a first step, in taking off substantially all of the part located on the same side of the overlayer 5 as the protective layer 3.

At the protective layer 3, the selective substance removal mode is at least one of the following selective substance removal modes:

- removal of the material of the overlayer 5 adjacent to the protective layer 3, the protective layer 3 forming a layer stopping the removal of substance;

- removal of material of the protective layer 3, the zone of the buffer structure I adjacent to the protective layer 3 forming a layer stopping the removal of substance.

Whatever the selective substance removal mode likely to be operated during recycling and intended to remove the remaining overlayer 5, there is a layer stopping the removal of substance (the protective layer 3 in the case of the first selective substance removal mode or the zone of the upper part of the buffer structure I, adjacent to the protective layer 3, in the case of the second selective substance removal mode), thus acting as a barrier to substance etching or attack, and in the same way protecting the material of the buffer structure I.

Furthermore, if may be advantageous that the protective layer 3 does not substantially disturb the crystallographic structure of the directly underlying buffer structure I, and does not disturb the crystalline growth of the overlying overlayer 5, in order to preserve the influence of the structure of the buffer structure I on the structure of the overlayer 5 being grown, and is therefore advantageously produced according to one of the three embodiments already discussed.

After the said removal of the substance overlying the buffer structure I, the recycling advantageously comprises producing a new overlayer 5, and possibly a new protective layer 3 in the case where the latter has been removed (during the second selective substance removal mode mentioned above or by a treatment suitable for removing this layer 3).

These layers 5 and 3 may be grown *in situ* or after a minor step of finishing the surface of the donor wafer 10 on which the growth(s) will take place, for example by CMP polishing, heat treatment or other smoothing techniques such that the dislocations and other defaults confined in the buffer structure I don't

propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

With reference to Figure 6, a third donor wafer 10 according to the invention differs mainly from the donor wafer 10 shown in Figure 3 by the fact that there is an interlayer 8 between the buffer structure I and the protective layer 3.

The composition and the crystallographic structure of this interlayer 8 will be chosen as a function of the physical, electrical and/or mechanical properties that it is desired to obtain.

The material of the interlayer 8 may, for example, have a nominal lattice parameter which is substantially identical to that of the buffer structure I in its part adjacent to its interface, so as to preserve a substantially relaxed structure. In this case, the interlayer 8 is an extension of the buffer structure I, which may for example further reinforce the crystallographic rigidity of the growth surface of the overlayer 5.

The material of this interlayer 8 may also have, for example, a nominal lattice parameter which is substantially different from that of the buffer structure I in the part adjacent to its interface, and have a thickness which is low enough to have to preserve the lattice parameter of the buffer structure I in its part adjacent to the protective layer 3, and thus be strained.

In an advantageous configuration, the interlayer 8 or the overlayer 5 is produced by layer growth, for example by CVD or MBE epitaxy.

In this configuration, and in a first case, the growth of the layer in question is carried out *in situ*, directly in continuation with the formation of the underlying layer, the latter in this case also advantageously being formed by layer growth.

In a second case, the growth of the layer in question is carried out after a minor step of finishing the surface of the upper surface of the underlying layer, for example, by CMP polishing, heat treatment or other smoothing techniques, such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

With regard to the protective layer 3, its role in this case is to protect virtually the entire underlying interlayer 8, the entire buffer structure I and the substrate 1 from the substance removal operated during the first recycling step.

At the protective layer 3, the selective substance removal mode is at least one of the following selective substance removal modes:

- removal of the material of the overlayer 5 adjacent to the protective layer 3, the protective layer 3 forming a layer stopping the removal of substance;

- removal of the material of the protective layer 3, the zone of the interlayer 8 adjacent to the protective layer 3 forming a layer stopping the removal of substance.

Whatever the selective substance removal mode likely to be operated during the recycling and intended to remove the remaining overlayer 5, there is a layer stopping the removal of substance (the protective layer 3 in the case of the first selective substance removal mode or the zone of the interlayer 8 adjacent to the protective layer 3, in the case of the second selective substance removal mode), thus acting as a barrier to substance etching or attack, and in the same way protecting the material of the buffer structure I.

Furthermore, it may be advantageous that the protective layer 3 does not substantially disturb the crystallographic structure of the directly underlying interlayer 8, and does not disturb the crystalline growth of the overlying overlayer 5, in order to preserve the influence of the structure of the interlayer 8 on the structure of the overlayer 5 being grown, and must therefore be produced according to one of the two embodiments already discussed.

After the said removal of the substance overlying the interlayer 8, the recycling advantageously comprises producing a new overlayer 5, and possibly a new protective layer 3 in the case where the latter has been removed (during the second selective substance removal mode mentioned above or by a treatment suitable for removing this layer 3).

These layers 5 and 3 may be grown *in situ* or after a minor step of finishing the surface of the donor wafer 10 on which the growth(s) will take place, for example, by CMP polishing, heat treatment or other smoothing techniques, performed such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

With reference to Figures 7a to 7f, the various steps are shown of a method

of taking off a thin layer from and of recycling a donor wafer 10 comprising a protective layer 3, which uses a donor wafer 10 with a layer structure substantially identical to that described above with reference to Figure 4 and which therefore comprises, with reference to Figure 7a, a substrate 1, and a buffer structure I within which there is a protective layer 3.

In the example which we will study, the protective layer 3 takes off a buffer layer 2 and an additional layer 4 in the buffer structure I.

In this exemplary method according to the invention, an overlayer 5 has been added above the additional layer 4.

The removal that will be carried out during this method will relate to taking off part of the additional layer 4 and of the overlayer 5.

In the same way and in other structural configurations of the donor wafer 10, there may be several overlayers and the taking-off would then relate to the overlayers and possibly part of the additional layer 4, or there may be no overlayer and the taking-off would then relate to only part of the additional layer 4.

Furthermore, it is often necessary to have a fairly thin protective layer 3: as already explained above, too thick a protective layer 3 could influence the crystalline properties of the buffer structure I, such as generating defects, for example dislocations, or changes in the lattice parameters.

For this, the thickness of the protective layer 3 must be less than a critical thickness beyond which the undesirable effects would be obtained in this case.

These four layers 2, 3, 4 and 5 have advantageously been formed by epitaxial growth according to known techniques, for example by CVD and MBE,

In a first case, at least one of these four layers is grown *in situ*, directly in continuation with the formation of the underlying growth support, the latter also being in this case advantageously formed by layer growth.

In a second case, at least one of these four layers is grown after a minor step of finishing the surface of the underlying growth support, for example by CMP polishing, heat treatment or other smoothing techniques, performed such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

A method of taking off a thin layer is shown in Figures 7b and 7c.

A first preferred taking-off step of the invention consists in creating a fragile zone in the additional layer 4, in order to carry out a subsequent detachment, and thus separate the desired layer(s).

Several techniques that can be operated to create such a fragile zone are presented here:

A first technique, called Smart-cut®, known to a person skilled in the art (and descriptions of which may be found in a number of works covering techniques for reducing wafers) consists, in its first step, in implanting atomic species (such as hydrogen ions) with a particular energy in order to create in this way a fragile zone.

A second technique consists in forming a fragile interface by creating at least one porous layer, as described for example in document EP-A-0 849 788.

The fragile zone advantageously formed according to one of these two techniques is, in this exemplary method according to the invention, created between the overlayer 5 and the additional layer 4 or in the additional layer 4.

Where the overlayer 5 is thick enough, the fragile zone may be formed therein. In particular, this is the case where the overlayer 5 consists of a stack of layers.

With reference to Figure 7b, a second step relating to taking off a thin layer consists in attaching a receiving substrate 6 to the surface of the overlayer 5.

The receiving substrate 6 forms a mechanical support which is rigid enough to support the overlayer 5 which will be taken off from the donor wafer 10, and to protect it from any mechanical strains coming from the outside.

This receiving substrate 6 may, for example, be made of silicon or of quartz or of another type of material.

The receiving substrate 6 is attached by placing it in intimate contact with the overlayer 5 and by bonding it thereon, in which molecular adhesion is advantageously carried out between the substrate 6 and the overlayer 5.

This bonding technique, together with variants, is in particular described in the document entitled "Semiconductor Wafer Bonding" (Science and technology, Interscience Technology) by Q.Y. Tong, U. Gösele and Wiley.

If necessary, the bonding is accompanied by a suitable pretreatment of the respective surfaces to be bonded and/or by a supply of heat energy and/or a supply

of an additional binder.

Thus, for example, heat treatment applied during or just after the bonding makes it possible to stiffen the bonded connections.

The bonding may also be controlled by a bonding layer, such as silica, inserted between the overlayer 5 and receiving substrate 6, having particularly high molecular bonding abilities.

Advantageously, the material forming the bonding face of the receiving substrate 6 and/or the material of the bonding layer possibly formed, is electrically insulating, in order to produce an SOI structure from the taken off layers the semiconductor layer of the SOI structure then being the overlayer 5 transferred with or without part of the additional layer 4.

Once the receiving substrate 6 is bonded, part of the donor wafer 10 is taken off at the fragile zone formed beforehand, by detaching it.

In the case of the said first technique (Smart-cut®), in a second step, the implanted zone (forming the fragile zone) is subjected to a heat and/or mechanical treatment, or other supply of energy, in order to detach it at the fragile zone.

In the case of the said second technique, the fragile layer is subjected to mechanical treatment or other supply of energy, in order to detach it at the fragile layer.

Detachment at a fragile zone according to one of these two techniques makes it possible to take off most of the wafer 10, in order to obtain a structure comprising possibly the rest of the buffer structure I, the overlayer 5, any bonding layer and the receiving substrate 6.

A step of finishing the surface of the structure formed, at the taken off layer, is then advantageously operated in order to take off any surface roughness, inhomogeneities in thickness and/or undesirable layers, by using, for example, chemical-mechanical polishing CMP, etching or at least a heat treatment.

A post-taking-off layer 7 forms the part, after taking-off, which remains above the protective layer 3, the entire wafer forming a donor wafer 10' to be sent for recycling in order to be reused subsequently during another layer taking-off.

The recycling steps are shown in Figures 7d, 7e and 7f.

With reference to Figure 7d, a first recycling step corresponds to removing

virtually all the post-taking-off layer 7 and possibly removing the protective layer 3.

Mechanical or chemical-mechanical attack or a suitable treatment may possibly and first of all be operated in order to remove part of the rest of the additional layer 4 of the post-taking-off layer 7, such as attack by grinding, polishing, CMP, chemical etching, heat treatment and smoothing performed such that the dislocations and other defaults confined in the buffer structure I don't propagate, don't increase in size and don't create any slip planes, stacking defaults or other defaults which can decrease the quality of the buffer structure I.

It is also possible for several of these material etching or attack techniques to be combined or to follow one another, such as for example a succession of attacks by chemical etching and by CMP.

In all cases, the first recycling step comprises using at least one of the selective substance removal modes discussed above.

With reference to Figures 7e and 7f, a second recycling step corresponds to the restoration of layers which are substantially identical to those which existed before taking-off, with the respective formations of an additional layer 4' and of an overlayer 5'.

Furthermore, the restoration comprises the formation of a protective layer 3 where the latter was removed.

The layers are advantageously restored by forming a layer according to a technique which is substantially identical to one of these detailed above.

The layers 4' and 5' obtained of the donor wafer 10''' are not necessarily identical to the layers 4 and 5 of the donor wafer 10, it being possible for the donor wafer shown in Figure 7d to act as a substrate for other types of layers.

In the exemplary method according the invention which has just been detailed, the taking-off relates to part of the additional layer 4 and the overlayer 5.

In parallel, this example may be applied to a taking-off concerning only part of the additional layer 4 (the donor wafer 10 not having an overlayer 5).

In parallel, this example may be applied to a taking-off concerning only part of the overlayer 5, and the recycling then comprises removing the remaining part of the overlayer 5.

In the exemplary method according to the invention which has just been

detailed, the protective layer 3 is located between the buffer layer 2 and additional layer 4.

Obviously, this example is applicable also to cases where the protective layer 3 is located in the buffer layer 2 or in the additional layer 4.

In general, this example extends to the case where the protective layer 3 is located in the buffer structure I.

The description of the method according to the invention with reference to Figures 7a to 7f using a donor wafer 10 shown in Figure 2 can also be easily transposed to donor wafers 10 shown in:

- Figure 5 by locating the protective layer 3 between the buffer structure I and the overlayer 5 instead of placing it within the buffer structure I, the layer then being taken off at the overlayer 5, the taking-off of the substance for recycling ending in selective etching of the overlayer 5 with respect to the protective layer 3 and/or in selective etching of the protective layer 3 with respect to the buffer structure I;

- Figure 6 by adding an interlayer 8 to the donor wafer 10 by locating it between the buffer structure I and the protective layer 3, the layer being taken off at the overlayer 5, the removal of substance for recycling ending in selective etching of the overlayer 5 with respect to the protective layer 3 and/or in selective etching of the protective layer 3 with respect to the interlayer 8.

After recycling the donor wafer 10 according to the invention, a method of taking off a useful layer can then be operated again.

Thus, in an advantageous context of the invention, a cyclic method of taking a useful layer off a donor wafer 10 according to the invention is operated, by making the following succeed each other repeatedly:

- a taking-off mode; and
- a recycling method according to the invention.

Before operating the cyclic taking-off method, it is possible to implement a method of producing the donor wafer 10 according to the invention with one or more of the techniques for producing thin layers on a substrate, described above.

In the remainder of this document, we present examples of configurations of donor wafers 10 comprising buffer structures I, and capable of being operated by a method according to the invention.

In particular, we will present materials which can advantageously be used in such donor wafers.

As we have seen, a buffer structure I produced on a substrate 1 having a first lattice parameter has, most of the time, the prime function of having a second lattice parameter on its free face.

Such a buffer structure I then comprises a buffer layer 2 making it possible to produce such matching of a lattice parameter.

The technique most often employed to obtain a buffer layer 2 having this property is to have a buffer layer 2 consisting of several atomic elements comprising:

- at least one atomic element which is in the composition of the substrate 1; and
- at least one atomic element, none or very little of which is in the substrate 1, having a concentration changing gradually within the thickness of the buffer layer 2.

The gradual concentration of this element in the buffer layer 2 will be the main cause of the gradual change of the lattice parameter in the buffer layer 2, in a metamorphic manner.

Thus, in this configuration, a buffer layer 2 will mainly be an alloy.

The atomic elements chosen for the composition of the substrate 1 and for the buffer layer 2 may be of type IV, such as Si or Ge.

For example, in this case, it is possible to have a substrate 1 made of Si and a buffer layer 2 made of SiGe with a Ge concentration changing progressively with thickness between a value close to 0 at the interface with the substrate 1 and a particular value on the other face of the buffer layer 2.

In another scenario, the composition of the substrate 1 and of the buffer layer 2 may comprise pairs of atomic elements of type III-V, such as the possible (Al,Ga,In)-(N,P,As) combinations.

For example, in this case, it is possible to have a substrate 1 made of AsGa and a buffer layer 2 comprising As and/or Ga with at least one other element, the latter element changing progressively with thickness between a value close to 0 at the interface with the substrate 1 and a particular value on the other face of the buffer layer 2.

The composition of the substrate 1 and of the buffer layer 2 may comprise pairs of atomic elements of type II-VI, such as the possible (Zn,Cd)-(S,Se,Te) combinations.

Below, we offer some examples of such configurations:

The first three examples particularly relate to donor wafers 10 comprising a substrate 1 made of Si and a buffer layer 2 made of SiGe and other layers of Si and of SiGe.

These wafers 10 are particularly useful in the case of taking off layers of strained SiGe and/or Si to produce SGOI, SOI or Si/SGOI structures.

In this context, the type of etching solutions used differ depending on the material (Si or SiGe) to be etched. Thus, etching solutions capable of etching these materials will be classed into categories, by attributing an identifier included in the following list to each category:

- S1: selective etching solutions for Si with respect to SiGe such as a solution comprising at least one of the following compounds: KOH, $NH_4OH$ (ammonium hydroxide), TMAH, EDP or $HNO_3$ or solutions currently being studied combining agents such as $HNO_3$, $HNO_2H_2O_2$, HF, $H_2SO_4$, $H_2SO_2$, $CH_3COOH$, $H_2O_2$ and $H_2O$, as explained in document W0 99/53539, page 9.
- S2: selective etching solutions for SiGe with respect to Si such as a solution comprising HF:$H_2O_2$:$CH_3COOH$ (selectivity of about 1:1000) or HNA (hydrofluoric-nitric-acetic solution).
- Sc1: selective etching solutions for SiGe having a Ge concentration substantially less than or equal to 20% with respect to SiGe having a Ge concentration approximately equal to or greater than 25%, such as a solution comprising TMAH or KOH.
- Sd1: selective etching solutions for undoped Si with respect to Si doped with boron, preferably at more than $2 \times 10^{19}$ $cm^{-3}$, such as a solution comprising EDP (ethylenediamine pyrocatechol), KOH or $N_2H_2$ (hydrazine).

<u>Example 1</u>: After recycling, the donor wafer 10 consists of:

- a substrate 1 made of Si;
- a buffer structure I made of SiGe with a buffer layer 2 and an additional

layer 4;

- a post-taking-off layer 7 made of Si or of SiGe which forms the rest of an overlayer 5 after taking off part of the latter.

The buffer layer 2 preferably has a Ge concentration progressively increasing from the interface with the substrate 1, in order to make the SiGe lattice parameter change as explained above.

The thickness is typically between 1 and 3 micrometers in order to obtain good structural relaxation at the surface, and to contain the defects associated with the difference in lattice parameter so that they are buried.

The additional layer 4 is made of SiGe substantially relaxed by the buffer layer 2, with a Ge concentration which is advantageously uniform and substantially equal to that of the buffer layer 2 near their interface.

The concentration of germanium in the silicon within the relaxed SiGe layer 4 is typically between 15% and 30%.

This limitation at 30% represents a typical limitation of the current techniques, but may be made to change in the next few years.

The additional layer 4 has a thickness which may vary hugely depending on the case, with a typical thickness of between 0.5 and 1 micron.

In the case where the post-taking-off layer 7 is made of Si, selective etching of the latter with respect to the additional layer 4 made of SiGe may advantageously be operated, with an S1-type etching solution, in order to take it off.

In the case where the post-taking-off layer 7 is made of SiGe and where:

- the Ge concentration in the post-taking-off layer 7 is substantially less than or equal to 20%, and

- the Ge concentration in the additional layer 4 is approximately equal to or greater than 25%,

selective etching of the post-taking-off layer with respect to the additional SiGe layer 4 will be operated, with an Sc1-type etching solution, in order to take it off.

In all cases, the last part of the post-taking-off layer 7 is thus completely removed by chemical means, with an etch-stop at the protective layer 3 which thus

forms a stop layer, protecting the underlying layers that it is desired to preserve.

Example 2: After recycling, the donor wafer 10 is substantially identical to that presented in example 1, with the exception of the presence of a protective layer 3 within the wafer 10.

The protective layer 3 consists of:

- strained Si; or
- SiGe; or
- boron-doped Si.

It will be recalled that in the case where the protective layer 3 is made of strained Si, the thickness of the protective layer 3 here must not exceed a critical thickness.

Thus, for example, for a protective layer 3 made of strained Si inserted between two SiGe layers respectively having a Ge concentration substantially equal to 20%, the critical thickness is typically equal to about 20 nanometres.

In a first case, the protective layer 3 is located between two SiGe layers.

This is especially the case where the protective layer 3 is located between two layers of the buffer structure I; or between the buffer structure I and a post-taking-off layer 7 made of SiGe; or in the post-taking-off layer made of SiGe.

Several types of etching may thus be operated depending on the material of the protective layer 3:

- If the protective layer 3 is made of strained Si:

  ✓ the overlying part made of SiGe is selectively etched with an S2-type solution;

  and/or:

  ✓ after having removed the post-taking-off layer 7, the protective layer 3 is selectively etched with an S1-type solution.

- If the protective layer 3 is made of SiGe with a Ge concentration approximately equal to or greater than 25% and if the overlying layer has a Ge concentration substantially less than or equal to 20%:

  ✓ the overlying SiGe part is selectively etched with an Sc1-type solution.

- If the protective layer 3 is made of SiGe with a Ge concentration

substantially less than or equal to 20% and if the underlying layer has a Ge concentration approximately equal to or greater than 25%:

✓ after having removed the post-taking-off layer 7, the protective layer 3 is selectively etched with an Sc1-type solution.

In a second case, the protective layer 3 is located between an underlying SiGe layer and an overlying Si layer.

This is especially the case if the protective layer 3 is located between the buffer structure I and a post-taking-off Si layer 7; or between an SiGe interlayer 8 and a post-taking-off Si layer 7; or in the post-taking-off layer 7 between an SiGe layer and an Si layer.

Several types of etching may then be operated depending on the material of the protective layer 3;

- If the protective layer 3 is made of B-doped Si:

✓ the overlying Si part is selectively etched with an Sd1-type solution;

- If the protective layer 3 is made of SiGe:

✓ the overlying Si part is selectively etched with an S1-type solution.

- If the protective layer 3 is made of SiGe with a Ge concentration substantially less than or equal to 20% and if the underlying layer has a Ge concentration approximately equal to or greater than 25%:

✓ after having removed the post-taking-off layer 7, the protective layer 3 is selectively etched with an Sc1-type solution.

In a third case, the protective layer 3 is located between two Si layers.

This is especially the case if the protective layer 3 is located between an Si interlayer and a post-taking-off Si layer 7; or in the post-taking-off Si layer 7.

Several types of etching may then be operated depending on the material of the protective layer 3:

- If the protective layer 3 is made of B-doped Si:

✓ the overlying Si part is selectively etched with an Sd1-type solution;

- If the protective layer 3 is made of SiGe:

✓ the overlying Si part is selectively etched with an S1-type

solution;

and/or

✓ after having removed the post-taking-off layer 7, the protective layer 3 is selectively etched with an S2-type solution.

Example 3: After recycling, the donor wafer 10 consists of:

- an Si substrate 1;

- a buffer structure I with an SiGe buffer layer 2 and an additional Ge layer 4;

- a post-taking-off AsGa layer 7 which forms the rest of an overlayer 5 after taking off part of the latter;

- a protective AlGaAs layer 3 placed in the post-taking-off layer 7.

The buffer layer 2 preferably has a Ge concentration increasing progressively from the interface with the substrate 1, in order to make the lattice parameter change between that of the Si substrate 1 and that of the additional Ge layer 4.

To this end, in the buffer layer 2, the Ge concentration is made to progress from about 0 to about 100%, or more precisely around 98%, for complete agreement of the theoretical lattice of the two materials.

In a first scenario, the selective chemical etching of the post-taking-off layer 7 with a selective etching solution, such as a solution comprising citric acid ($C_6H_8O_7$) and hydrogen peroxide having a pH between about 6 and 7 (the selectivity coefficient typically being 20), makes it possible to take off substantially all of the remaining post-taking-off layer 7, the protective layer 3 behaving here like an etch-stop layer.

In a second scenario, after removing part of the post-taking-off layer 7 overlying the protective layer 3, and for an aluminium concentration in the protective layer 3 greater than 20%, selective chemical etching of the protective layer 3 with a selective etching solution, such as a solution comprising diluted hydrofluoric acid (between about 9% and 48%) (the selectivity coefficient typically being between 350 and 10000), makes it possible to take off virtually all of the protective layer 3, the underlying post-taking-off layer 7 behaving here like an etch-stop layer.

In a third scenario, it is possible to make two selective etchings succeed each other in order to remove at least part of the post-taking-off layer 7 and to remove the protective layer 3.

The buffer structure I is thus preserved and is completely recycled.

Example 4: After recycling, the donor wafer 10 consists of:

- a substrate 1 comprising at least one AsGa part at its interface with the buffer structure I;

- at least part of a buffer structure I made of a III-V material;

- a post-taking-off layer 7 comprising a III-V material which constitutes the rest of an overlayer 5 after taking-off of part of the latter.

The prime benefit of this buffer structure I is to match the lattice parameter of the material of the overlayer 5 (whose nominal value is about 5.87 angströms) to that of the AsGa (whose nominal value is about 5.65 angströms).

In the bulk III-V materials, and by comparing bulk InP to bulk AsGa, the latter is less expensive, more widely available on the semiconductor market, less fragile mechanically, a material from which the use of technologies with contact by a rear face is better known, and whose size may reach high values (typically 6 inches instead of 4 inches for bulk InP).

All the benefits which can be offered by such a donor wafer 10 is therefore seen here: this is because it makes it possible to produce an active layer of a III-V material to be transferred with a particular quality and particular properties, which may for example be close to properties that would have been found when producing the latter material in bulk.

In a particular configuration of the donor wafer 10 before taking-off, the overlayer 5 before taking-off comprised InP to be taken off.

Since the bulk InP has a dimension generally limited to 4 inches, the donor wafer 10 gives, for example, a solution to producing an InP layer dimensioned at 6 inches.

A buffer structure I for producing such an overlayer 5 requires a thickness typically greater than one micron, and which will be made to change towards greater thicknesses, especially if it can be recycled according to the present

invention.

The epitaxial growth technique usually operated to produce such a buffer structure I is furthermore particularly difficult and expensive, it is therefore beneficial to be able to recover it at least partially after taking off the useful layer.

Advantageously, the buffer structure I comprises a buffer layer 2 consisting of InGaAs with an In concentration changing between 0 and about 53%.

The buffer structure I may further comprise an additional layer 4 made of a III-V material, such as InGaAs or InAlAs, with a substantially constant concentration of the atomic elements.

In a particular taking-off case, the InP overlayer 5 and part of the additional layer 4 will be taken off in order to transfer it to a receiving substrate.

Thus it will be possible to profit from any electrical or electronic properties existing between the two taken off materials.

This is the case, for example, if the part of the additional layer 4 taken off is made of InGaAs or of InAlAs: electronic band discontinuities between the latter material and InP create improved electronic mobilities in the taken off layers.

Other configurations of the donor wafers 10 are possible, comprising other III-V compounds, such as InAlAs or the like.

Typical applications of such layer taking-off are HEMT or HBT ("High-Electron Mobility Transistor" and "Heterojunction Bipolar Transistor", respectively) production.

Chemical etching solutions, which may be selective, suitable for removing some III-V materials with respect to other III-V materials will advantageously be used during the first recycling step.

Thus, for example, in order to remove an InP post-taking-off layer 7 without removing an underlying InGaAs layer, selective etching of InP will advantageously be operated with a solution comprising concentrated HCl.

<u>Example 5</u>: After recycling, the donor wafer 10 consists of:

- a substrate 1 comprising AsGa at its interface with the buffer structure I;

- a buffer structure I comprising InGaAs at its interface with the post-taking-off layer 7;

- an InP post-taking-off layer 7 which forms the rest of an overlayer 5 after

taking off part of the latter;

- a protective layer 3 made of $In_xGa_{1-x}As_yP_{1-y}$ placed between the post-taking-off layer 7 and the buffer structure I; or in the post-taking-off layer 7.

This type of donor wafer 10 (without the protective layer 3) has already been described in example 4.

In a first scenario, the selective chemical etching of the post-taking-off layer 7 with a selective etching solution, such as a solution comprising HF, makes it possible to take off virtually all of the remaining post-taking-off layer 7, the protective layer 3 behaving here like an etch-stop layer.

In a second scenario, after removal of the part of the post-taking-off layer 7 overlying the protective layer 3, the selective chemical etching of the protective layer 3 with a selective etching solution, such as a solution comprising $Ce^{IV}$ $H_2SO_4$, makes it possible to take off virtually all of the protective layer 3, the layer underlying the protective layer 3 behaving here like an etch-stop layer.

In a third scenario, it is possible to make two selective etchings succeed one another in order to remove at least part of the post-taking-off layer 7 and to remove the protective layer 3.

The buffer structure I is thus preserved and is completely recycled.

Example 6: After recycling, the donor wafer 10 comprises:

- a substrate 1 comprising AsGa at its interface with the buffer structure I;
- a buffer structure I comprising InGaAs;
- an InP protective layer 3 located on or in the InGaAs.

In a first scenario, the selective chemical etching of the InGaAs overlying the protective layer 3 with a selective etching solution, such as a solution comprising $Ce^{IV}$ $H_2SO_4$, makes it possible to take off virtually all of this material overlying the protective layer 3, the protective layer 3 behaving here like an etch-stop layer.

In a second scenario, after removing the InGaAs overlying the protective layer 3, the selective chemical etching of the protective layer 3 with a selective etching solution, such as a solution comprising HF, makes it possible to take off

virtually all of the protective layer 3, the InGaAs underlying the protective layer 3 behaving here like an etch-stop layer.

In a third scenario, it is possible for two selective etchings to succeed one another in order to remove part of the InGaAs and to remove the protective layer 3.

In the semiconductor layers presented in this document, other components may be added to them, such as carbon with a carbon concentration substantially less than or equal to 50% or more particularly with a concentration less than or equal to 5% in the layer in question.

Finally, the present invention is not limited to a buffer structure I, an intermediate layer 8 or an overlayer 5 made of materials presented in the examples above, but extends also to other types of alloys of IV-IV, III-V, II-VI type.

It should be specified that these alloys may be binary, ternary, quaternary or of a higher degree.

The present invention is not limited either to a recyclable buffer layer 2 or buffer structure I having the prime function of matching the lattice parameter between two adjacent structures with different respective lattice parameters, but also relates to any buffer layer 2 or buffer structure I as defined in the most general manner in the present document and which can be recycled according to the invention.

The structures finally obtained after taking-off are not limited either to SGOI, SOI, Si/SGOI structures, or to structures for HEMT and HBT transistors.

## CLAIMS

**1.** 1. Method of recycling a donor wafer (10) after having taken off at least one useful layer of a material chosen from semiconductor materials, the donor wafer (10) comprising successively a substrate (1), a buffer structure (I) and, before taking-off, a useful layer, the method comprising removal of substance on the side of the donor wafer (10) where the taking-off took place, characterized in that, after removal of substance, at least a part of the buffer structure (I) remains, this at least part of the buffer structure (I') can then be reused as a buffer structure (I) for a subsequent useful layer taking-off.

**2.** Method of recycling according to the preceding claim, characterized in that, before taking-off, the buffer structure (I) comprises a buffer layer (2) and an additional layer (4), the additional layer (4) having :

- a thickness which is great enough to contain defects; and/or
- a surface lattice parameter which is substantially different from that of the substrate (1).

**3.** Method of recycling according to one of the preceding claims, characterized in that the removal of substance comprises the removal of part of the buffer structure (I) remaining after the taking-off.

**4.** Method of recycling according to Claim 2, characterized in that the removal of substance comprises the removal of at least part of the additional layer (4) remaining after taking-off.

**5.** Method of recycling according to Claim 1 or 4, characterized in that the removal of substance comprises the removal of part of the buffer layer (2).

**6.** Method of recycling according to one of the preceding claims, characterized in that, before taking-off, the donor wafer (10) comprised an overlayer (5) which comprised the useful layer to be taken off, and in that, after taking-off, the removal of substance comprises the removal of the remaining overlayer (5).

**7.** Method of recycling according to the preceding claim, characterized in that the thickness of the overlayer (5) has been chosen so that, after taking-off, standard

mechanical means for removing substance, such as polishing means, can be operated on this overlayer (5) during the removal of substance, without removing substance from the buffer structure (I).

**8.** Method of recycling according to the claims 2 and 6, characterized in that the thickness of the overlayer (5) and the thickness of the additional layer (4) have been chosen so that, after taking-off, standard mechanical means for removing substance, such as polishing means, can be operated on this overlayer (5) and on this additional layer (4) during the removal of substance, without removing substance from the buffer layer (2).

**9.** Method of recycling according to one of the preceding claims, characterized in that the removal of substance comprises chemical etching.

**10.** Method of recycling according to one of the preceding claims, characterized in that the removal of substance from the donor wafer (10) comprises selective chemical etching.

**11.** Method of recycling according to the claim 2, characterized in that the removal of substance from the donor wafer (10) comprises a selective chemical etching of the material included in at least part of the additional layer (4) relative to the buffer layer (2).

**12.** Method of recycling according to Claim 6, characterized in that the removal of substance from the donor wafer (10) comprises a selective chemical etching of the first material included in the remaining overlayer (5) relative to the buffer structure (I).

**13.** Method of recycling according to the preceding claim, characterized in that the donor wafer (10) comprises:

- a substrate (1) of Si;
- a buffer structure (I) comprising an $Si_{1-x}Ge_x$ buffer layer (2) with a Ge concentration x increasing with thickness between 0 and a y value, and an $Si_{1-y}Ge_y$ layer (4) relaxed by the buffer layer (2).

**14.** Method of recycling according to the preceding claim combined with one of the Claims 6 to 8, characterized in that the overlayer (5) comprises SiGe and/or strained Si.

**15.** Method of recycling according to the claim 13 combined with one of the claims 6 to 8, characterized in that y=1, and in that the overlayer (5) comprises AsGa and/or Ge.

**16.** Method of recycling according to claim 1, characterized in that a protective layer (3) is further present in the donor wafer (10) so that at least a part of the buffer structure (I) underlies it; the material of the protective layer (3) being chosen from crystalline materials such that means for removing substance has an etching power which is substantially different for the material of the protective layer (3) than for the material of at least one of the two adjacent zones, and thus is able to operate a selective removal of substance.

**17.** Method of recycling according to the preceding Claim, characterized in that the nominal lattice parameter of the material of the protective layer (3) is substantially different from the lattice parameter of its underlying layer, and in that the protective layer (3) is thin enough to be mainly elastically strained by the underlying layer.

**18.** Method of recycling according to one of the two preceding claims, characterized in that the protective layer (3) is in the buffer structure (I).

**19.** Method of recycling according to claim 16 or 17 and Claim 2, characterized in that the protective layer (3) is in the buffer layer (2).

**20.** Method of recycling according to claim 16 or 17 and Claim 2, characterized in that the protective layer (3) is between the buffer layer (2) and the additional layer (4).

**21.** Method of recycling according to claim 16 or 17 and Claim 2, characterized in that the protective layer (3) is in the additional layer (4).

**22.** Method of recycling according to one of Claims 16 and 17, characterized in that the protective layer (3) overlies the buffer structure (I).

**23.** Method of recycling according to the preceding claim, characterized by an operation of a selective removal of material of the zone overlying the protective layer (3), the protective layer (3) being thus a stop-layer to this removal of

substance.

**24.** Method of recycling according to one of the two preceding claims, characterized by an operation of a selective removal of the material of the protective layer (3), the zone underlying it being thus a stop-layer to the removal of substance.

**25.** Method of recycling according to one of the two preceding claims, characterized in that the selective removal of substance at or near the protective layer (3) comprises selective mechanical attack; the material of the protective layer (3) being chosen from crystalline materials such that mechanical means has an attack power substantially different for the material of the protective layer (3) than for the material of at least one of the two adjacent zones and thus is able to operate a selective mechanical attack.

**26.** Method of recycling according to the preceding claim, characterized in that the selective mechanical attack is a polishing, possibly combined with the action of an abrasive and/or chemical etching.

**27.** Method of recycling according to one of the claims 23 and 24, characterized in that the selective removal of substance at or near the protective layer (3) comprises a selective chemical etching; the material of the protective layer (3) being chosen from crystalline materials such that one etching fluid has an etch power substantially different for the material of the protective layer (3) than for the material of at least one of the two zones adjacent to the protective layer (3) and thus is able to operate a selective etching.

**28.** Method of recycling according to the preceding claim, characterized in that a mechanical attack of the protective layer (3) is operated in combination with the selective chemical etching so as to implement a selective chemical-mechanical planarization.

**29.** Method of recycling according to the preceding claim or to one of the claims 10 to 12, characterized in that the etch selectivity between the etched material and the stop material which "stops" etching, is obtained by employing determinated etch chemical species and by the fact that:

- the two materials are different; or
- one of the two materials is doped; or

- the two materials are substantially identical, but at least one atomic element in one material has an atomic concentration which is substantially different from that of the same atomic element in the other material; or
- the two materials have different porosity densities.

**30.** Method of recycling according to the preceding claim, characterized in that the etched material and the stop material are together one of the following double-materials set :

| etched material | stop material |
|---|---|
| Si | doped Si |
| Si | SiGe |
| SiGe | Si |
| $Si_{1-x}Ge_x$ | $Si_{1-y}Ge_y$ , with $y \neq x$ |

**31.** Method of recycling according to one of the preceding claims, characterized in that it further comprises a step of finishing the surface of the donor wafer (10) after the step of removing substance from the donor wafer (10).

**32.** Method of recycling according to one of the preceding claims, characterized in that it further comprises, after the step of removing substance from the donor wafer (10), a step of forming layer on the side of the donor wafer (10) where the removal of substance took place, so as regenerating the donor wafer (10).

**33.** Method of recycling according to the preceding claim and one of the claims 4 and 5, characterized in that the step of forming layer comprises an operation of forming a new part of the buffer structure (I) above the remaining part of the buffer structure (I').

**34.** Method of recycling according to one of the two preceding claims and to one of the claims 6 to 8, characterized in that the step of forming layer comprises an operation of forming an overlayer (5) on the donor wafer (10) so as to form at least one new useful layer to be subsequently taken off.

**35.** Method of recycling according to one of the three preceding claims, characterized in that the step of forming layer comprises an operation of forming in the donor wafer (10) a new protective layer (3) according to claim 16.

**36.** Method of recycling according to one of the four preceding Claims, characterized in that layer(s) is formed during the step of forming layer by crystal growth.

**37.** Method of recycling according to one of the preceding claims, characterized in that the donor wafer (10) comprises at least one layer further comprising carbon at a concentration substantially less than or equal to 50%.

**38.** Method of recycling according to one of the preceding claims, characterized in that the donor wafer (10) comprises at least one layer further comprising carbon at a concentration substantially less than or equal to 5%.

**39.** Method of producing a donor wafer (10) intended to provide a useful layer by taking-off and capable of being recycled after taking-off according to the method of recycling according to one of the claims 16 to 28, characterized in that it comprises the following steps:

-formation of a first part (2') of a buffer structure (I) on a substrate (1);

-formation of a protective layer (3) on the first part (2') of the buffer structure (I), in a material chosen from crystalline materials;

-formation on the protective layer (3) of the second part (4') of the buffer structure (I), such that it has a lattice parameter in the vicinity of the protective layer (3) substantially the same as that of the first part (2') of the buffer structure (I) in the vicinity of the protective layer (3).

**40.** Method of producing a donor wafer (10) according to the preceding claim, characterized in that the buffer structure comprising :

- a buffer layer (2) ; and
- an additional layer (4) having a thickness great enough to contain defects;

characterized in that the protective layer (3) is formed:

- in the buffer layer (2), during its formation, or
- between the buffer layer (2) and the additional layer (4), or
- in the additional layer (4), during its formation.

**41.** Method of producing a donor wafer (10) according to the claim 39 or 40, characterized in that it further comprises the formation of an overlayer (5) on the buffer structure (I) so as to form at least one useful layer.

**42.** Method of producing a donor wafer (10) being intended to supply a useful layer by taking-off and capable of being recycled after taking-off according to one of Claims 16 to 28, characterized in that it comprises the following steps:

-formation of a buffer structure (I) on a substrate (1);

-formation of a protective layer (3) on the buffer structure (I) with a material chosen from crystalline materials;

-formation of an overlayer (5) on the protective layer (3).

**43.** Method of producing a donor wafer (10) according to one of the four preceding claims, characterized in that the thickness of the protective layer (3) is controlled during its formation such that the formed protective layer (3) is thin enough to be substantially elastically strained by its underlying layer.

**44.** Method of producing a donor wafer (10) according to one of the five preceding claims, characterized in that the formation of the protective layer (3) is a crystal growth.

**45.** Method of producing a donor wafer (10) according to the preceding claim, characterized in that it further comprises an operation of doping the protective layer (3) such that it becomes a stop-layer of a removal of its overlying layer material.

**46.** Method of producing a donor wafer (10) according to the claim 44, characterized in that it further comprises an operation of porosification of the protective layer (3) such that its underlying layer becomes a stop-layer of its removal.

**47.** Method of taking off a useful layer on a donor wafer (10) in order to be transferred to a receiving substrate (6), characterized in that it comprises:

(a) bonding the donor wafer (10) to the receiving substrate (6);

(b) detaching a useful layer bonded to the receiving substrate (6) from the donor wafer (10),

(c) recycling the donor wafer complying with the method of recycling according to one of the claims 1 to 38.

**48.** Method of taking off a useful layer according to the preceding claim, characterized in that it comprises, before step (a), a step of forming a bonding

layer.

**49.** Method of taking off a useful layer according to one of the three preceding claims, characterized in that:

- it further comprises, before step (a), a step of implanting atomic species through the surface of the donor wafer (10) neighbouring the buffer structure (I) at a determinate depth, in order to form a fragile zone at this depth; and in that :
- the step (b) is operated by supplying energy to the donor wafer (10) in order to detach a structure comprising the receiving substrate (6) and the useful layer at the fragile zone level.

**50.** Method of taking off a useful layer according to one of the claim 48, characterized in that :

- it further comprises, before step (a), a step of forming by porosification a layer in the donor wafer (10) followed by a growth of a layer (which will become the useful layer after detaching of step (b)), the porosified layer forming a fragile zone inside or above the buffer structure (I); and in that :
- the step (b) is operated by supplying energy to the donor wafer (10) in order to detach a structure comprising the receiving substrate (6) and the useful layer at the fragile zone level.

**51.** Method of taking off a useful layer according to one of Claims 47 to 50, characterized in that the useful layer detached during step (b) comprises part of the buffer structure (I).

**52.** Method of cyclically taking off a useful layer from a donor wafer (10), characterized in that it comprises several steps of taking off a useful layer, each of these steps complying with the method of taking-off according to one of Claims 47 to 51.

**53.** Application of the method of cyclically taking-off according to the preceding claim or of the method of taking-off according to one of Claims 47 to 51, for producing a structure comprising the receiving substrate (6) and the useful layer, the useful layer comprising at least one of the following materials:
SiGe, Si, an alloy belonging to the III-V family, the composition of which is respectively chosen from the possible (Al,Ga,In)-(N,P,As) combinations.

**54.** Application of the method of cyclically taking-off according to the Claim 52 or of the method of taking-off according to one of Claims 47 to 51, for producing semiconductor-on-insulator structure, a such structure comprising the receiving substrate (6) and the useful layer.

**55.** Donor wafer (10) having supplied a useful layer by taking-off and capable of being recycled according to one of Claims 1 to 38, characterized in that it successively comprises a substrate (1) and a remaining part of the buffer structure (I).

**56.** Donor wafer (10) recyclable according to the method of recycling according to one of Claims 16 to 28, characterized in that a protective layer (3) is present in the buffer structure (I).

**57.** Donor wafer (10) according to the preceding claim, characterized in that, before taking-off, the buffer structure (I) comprises a buffer layer (2) and an additional layer (4), the additional layer (4) having:

- a thickness which is large enough to contain defects; and/or
- a surface lattice parameter which is substantially different from that of the substrate (1);

and in that the protective layer (3) is located:

- in the buffer layer (2); or
- between the buffer layer (2) and the additional layer (4); or
- in the additional layer (4).

**58.** Donor wafer (10) recyclable complying with the method of recycling according to one of Claims 16 to 28, characterized in that a protective layer (3) overlies the buffer structure (I).

**59.** Donor wafer (10) according to one of the three preceding claims, characterized in that it further comprises an overlayer (5) on the buffer structure (I) so as to comprise at least one useful layer.

**60.** Donor wafer (10) according to one of the four preceding Claims, characterized in that the protective layer (3) is substantially elastically strained by its underlying layer.

**61.** Donor wafer (10) according to one of the five preceding Claims, characterized in that the protective layer (3) is doped.

**62.** Donor wafer (10) according to the six preceding Claims, characterized in that the protective layer (3) is made of a porous material.

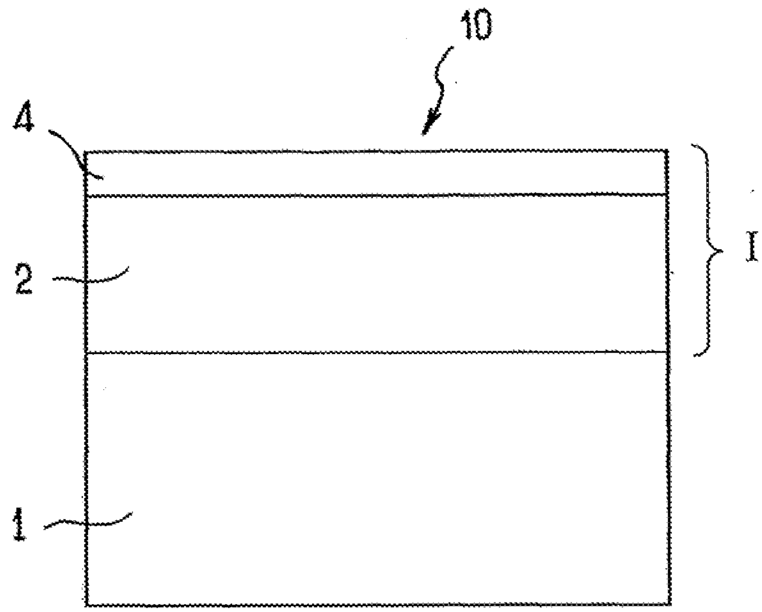


FIG.1

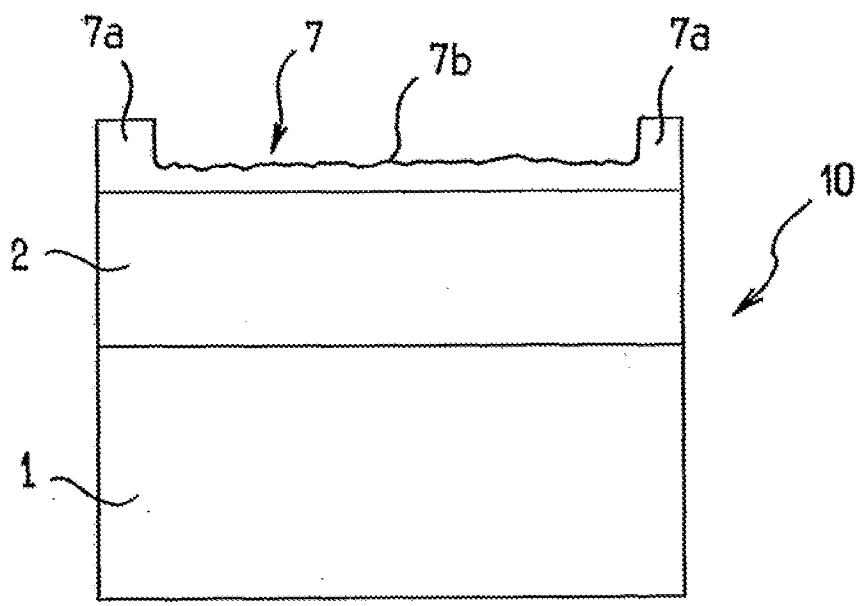


FIG.2

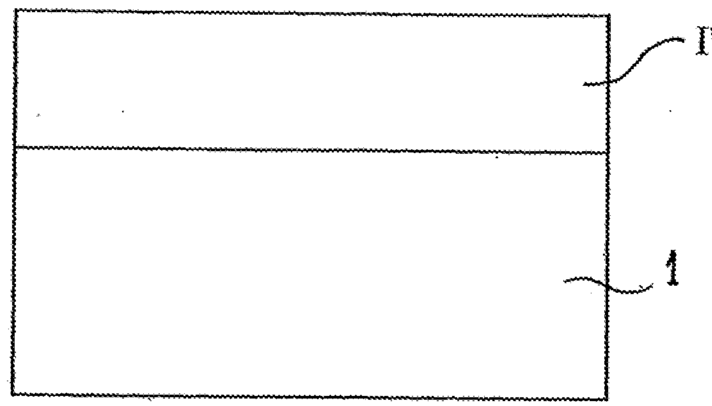


FIG.3

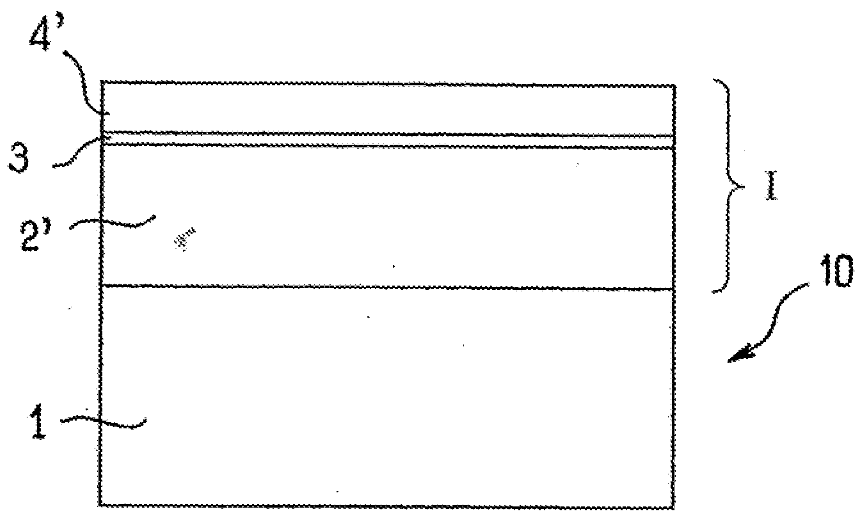


FIG.4

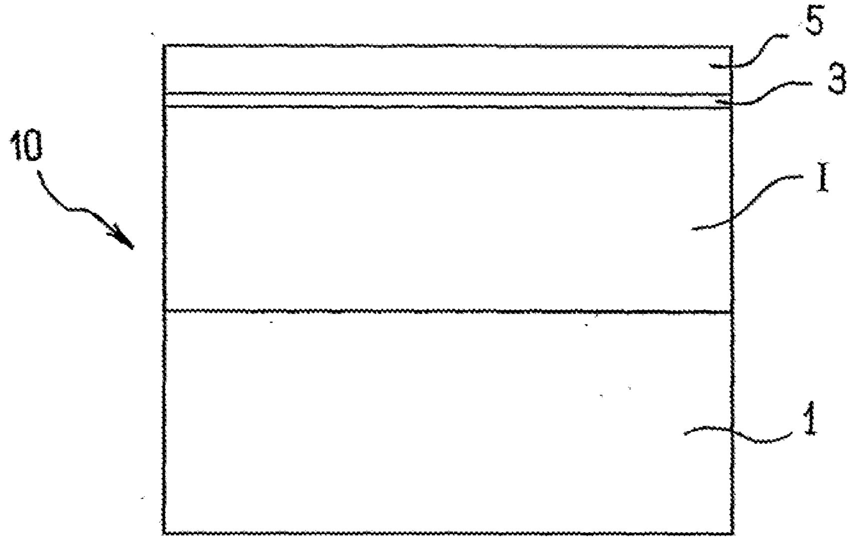


FIG.5

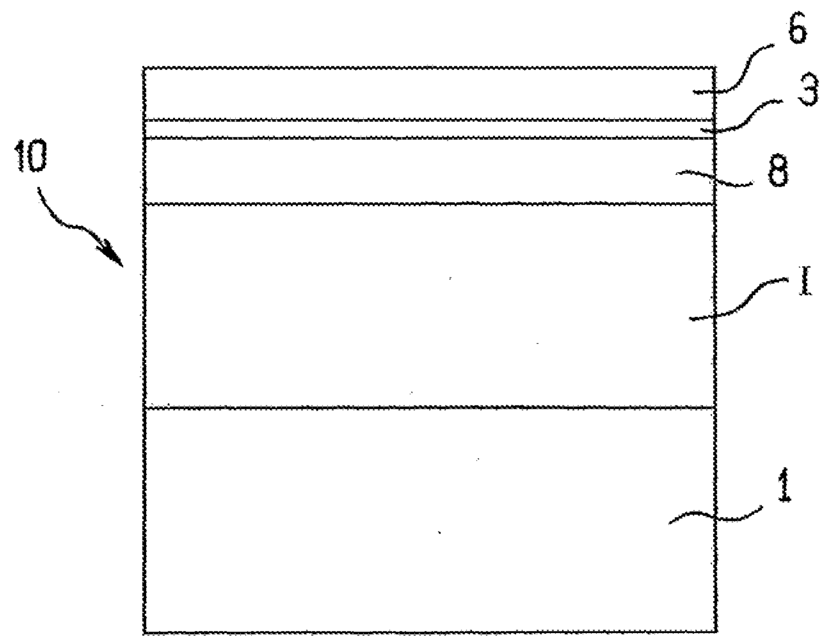


FIG.6

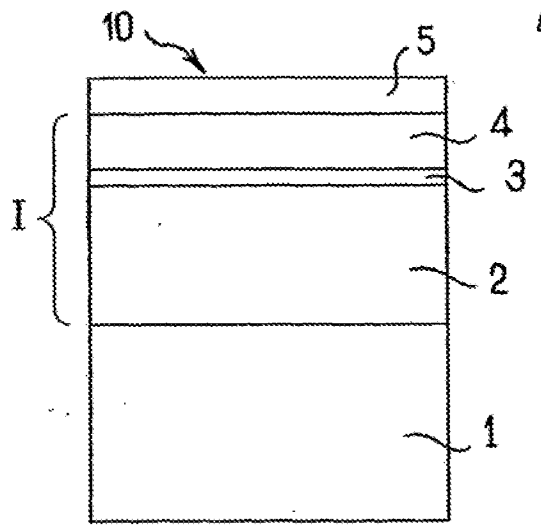


FIG.7a

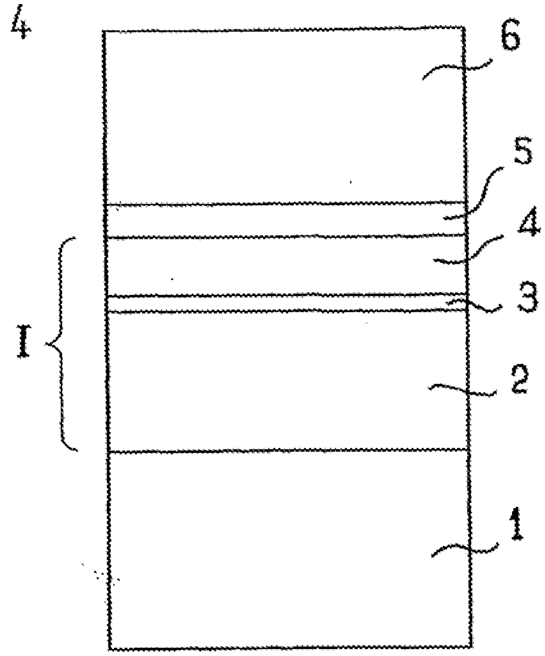


FIG.7b

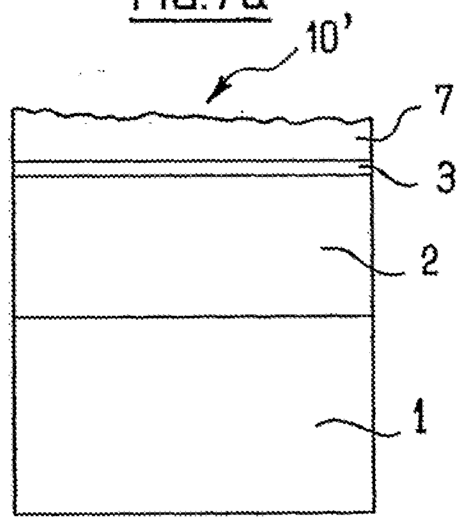


FIG.7c

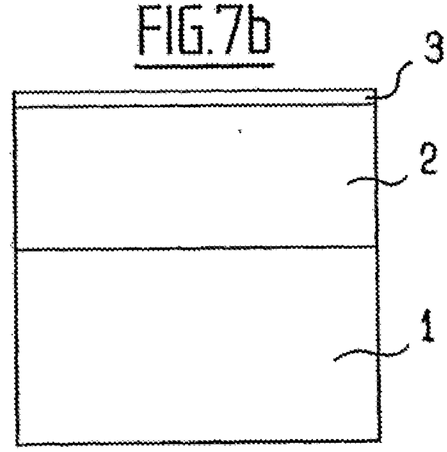


FIG.7d

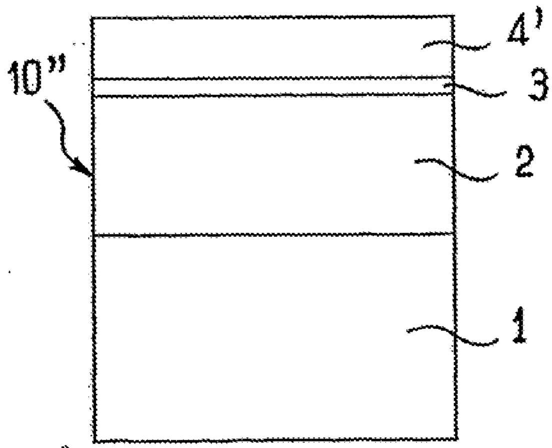


FIG.7e

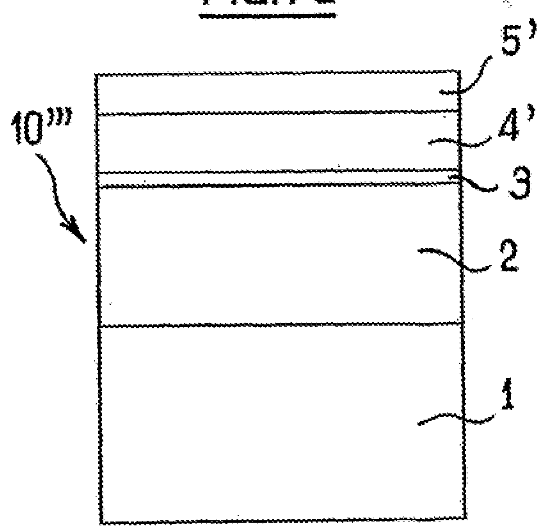


FIG.7f

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Title:

# 2 Bit Cell Eeprom Cell using Band to Band Tunneling for Data Read Out.

Text

TDB

Disclosed is a new non-volatile memory cell that stores 2 bits of data in each MOSFET. The cell uses channel hot-electron injection for writing, band to band tunnel injection of holes or electron detrapping for erasing, and band to band tunneling for data readout. The cell is especially well-suited for dense memories, which require a small number of read and write cycles.

In usual electrically alterable memory cells (EEPROMs), the state of the memory cell is read by detecting changes in the channel current of a MOSFET, due to charges that are trapped either in a floating gate or in traps inside the gate insulator. Instead of the channel current, in the disclosed cell changes in the reverse bias tunnel current of the source and drain junctions are used to read the stored data.

Indeed, in NMOSFETs biased under accumulation (Fig. 1) so that a hole accumulation layer 1 exists, a p+/n+ tunnel diode exists at the source 2 and drain 3 (1). The reverse bias tunnel current 4,5 through these diodes is very sensitive to the electric field in the gate-oxide around the drain and source junctions (2). If electrons are injected above either the source or drain junction, part of them are trapped in the gate oxide 6 and modify the electric field, and hence the current through the associated tunnel diode. Therefore, the presence or absence of electrons in the oxide above the two source/drain junctions can be used to store 2 bits in each MOSFET.

The cell is made using the same fabrication steps as for an ordinary NMOSFET, but the gate insulator must be optimized for enhanced electron trapping, but low detrapping rate. Oxide nitride oxide (3) may be used.

Fig. 2 shows the two bits of the cell under typical operating conditions.

During WRITE (Figs. 2a, 2b), hot-electrons are heated and injected into the oxide on the cell side on which a high voltage is applied. The other half of the NMOSFET is unaffected by these biasing conditions. The injected electrons modify the electric field only around the injecting junction.

During READ of the data (Figs. 2c, 2d), a negative gate voltage and reverse (positive) junction voltage are applied on the selected half-device, so that a band to band tunnel current flows from the n+ zone to the substrate. Since this current is very sensitive to the electric field configuration only around the junction, its value indicates whether electrons have been injected in the half-cell or not, hence the state of the stored bit. During readout, both the gate and drain voltages should be kept to the smallest value necessary to obtain a sufficient readout current (necessary to discharge parasitic capacitors, hence achieve sufficient speed), but to avoid electron detrapping or hole injection during the readout process,

which would destroy the stored data (see below).

ERASING of the cell occurs by applying the same voltages as for readout, but with higher amplitudes (Figs. 2e, 2f), in order to detrap the trapped electrons by FN injection from the traps. If the drain voltage is high enough, holes that are left by electrons that tunnel from the valence band to the conduction band in the drain are heated and may be injected into the oxide. This injection will lead to the disappearance of the trapped electrons, hence also to the erasure of the cell, but may also produce some interface states which will decrease the lifetime of the cell. Therefore, the drain voltage should not be too high during erase.

Since the active device is contained in the gate-drain overlap region, the distance between the source and drain regions can be made as small as is practically achievable. However, a minimum distance has to be maintained, otherwise during WRITE, electron injection from one-half of the cell may program the other half. The minimum width of the device is limited by the readout current necessary to achieve the required speed.

Fig. 3A shows the virtual ground matrix arrangement of the cells, and Fig. 3B a possible layout. The driving/decoding circuit is not special, except that the word line drivers must be able to provide a negative potential. However, since no static current is drawn from them, this voltage can easily be generated on-chip. Therefore this cell is well adapted for 5V-only memory chips.

Fig. 4 shows the results of a test measurement on an ordinary NMOSFET with an ONO gate oxide, which proves the validity of the concept. The voltages used were: Vg = +5V, Vd = +5V for programming, Vg = -4V, Vd = +4V for erasing, Vg = -2V, Vd = +2V for readout, and the write/erase times were one second. Much shorter programming and erase times are probably achievable (around 10ms, depending on applied voltages), but are not shown here. After 45 write/erase cycles, a "write" pulse was applied at T = 90s, and the readout current monitored to check data retention. A quite important initial detrapping occurs, but gradually slows down. A similar phenomenon occurs after the "erase" pulse, which is after about 20,000s in Fig. 4. The initial detrapping rate should be minimized by optimizing the thickness of the O,N and O layers (4).

Since the readout speed of the cell is somewhat limited by the parasitic capacitance and the small readout current, this cell is especially suitable for high density lower performance memory arrays. Therefore, it is especially well-suited as a non-volatile storage in solid-state hard-disk replacement, where data are stored in a RAM when the power is on, and are quickly transferred to the non-volatile memory before the power goes out. In this application, speed is not a major concern and density/cost is of prime importance. Higher speed can be achieved if a low current sensing scheme is devised.

References (1) S. R. Hofstein, G. Warfield, "The insulated gate junction triode," IEEE ED-12, 66 (1965). (2) A. Acovic, M. Ilegems, "Characterization of degradation due to hot-carriers in MOSFETs by the drain-substrate gate controlled tunnel diode," in extended proceedings ESSDERC'87, 265 (1988). (3) Y. Kamigaki, S. Minami, T. Hagiwara, K. Furusawa, T. Furuno, K. Uchida, M. Terasawa, K. Yamazaki, "Yield and reliability of MNOS EEPROM products," IEEE JSSC-24, 1714 (1989). (4) S. Minami, Y. Kamigaki, K. Uchida, K. Furusawa, T. Hagiwara, "Improvement of written-state retentivity by scaling down MNOS memory devices," Japan J. Appl. Phys. 27, part 2, p. L 2168 (1988).

Diagrams:

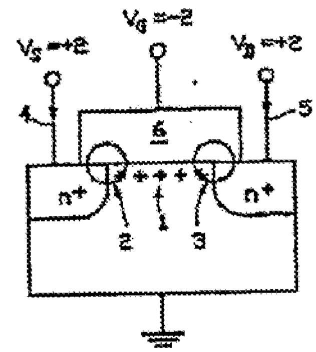



FIG.1
PRINCIPLE OF THE DISCLOSED EEPROM CELL

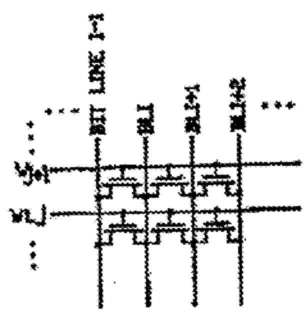



FIG.3A
ARRAY OF CELLS

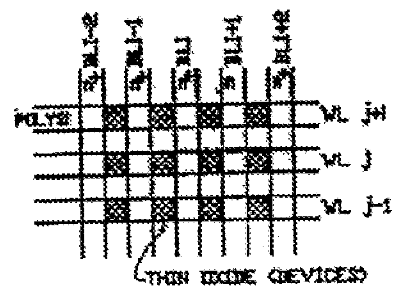



FIG.3B SCHEMATIC LAYOUT

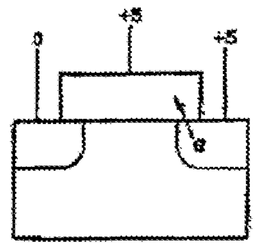



FIG.2a WRITE BIT 1

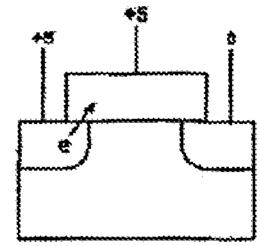



FIG.2b WRITE BIT 2

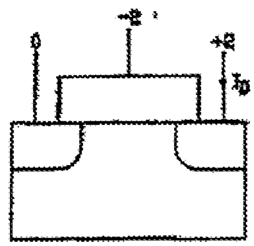



FIG.2c READ BIT 1

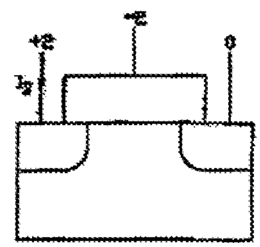



FIG.2d READ BIT 2

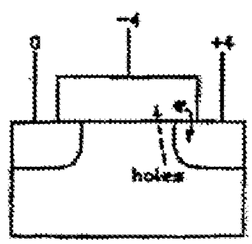



FIG.2e ERASE BIT 1

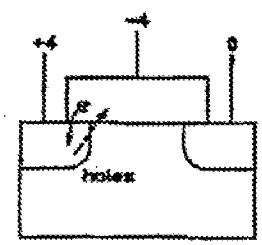
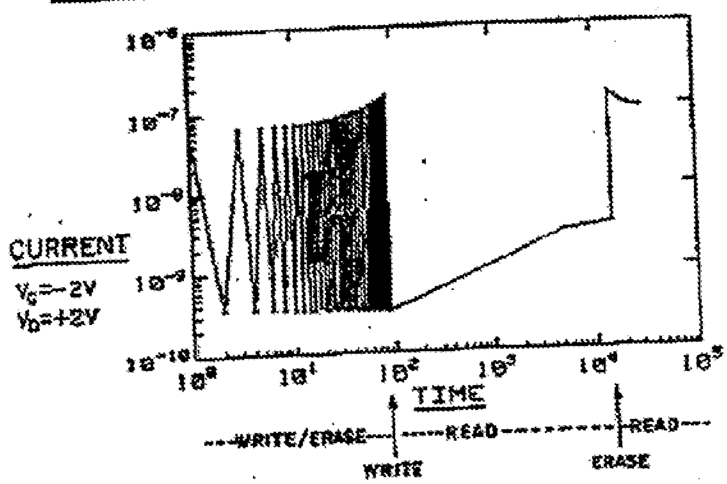



FIG.2f ERASE BIT 2

FIG.4 EXPERIMENTAL VERIFICATION



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C2

# Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors

Mark A. Armstrong[1], Dimitri A. Antoniadis[1], A. Sadek[2], K. Ismail[2,3] and Frank Stern[*,3]

[1]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139

[2]Dept. of Electronics and Communications, Faculty of Engineering, Cairo University, Giza, Egypt

[3]IBM T. J. Watson Research Center, Yorktown Heights, NY 10598

### Abstract

A design is presented and computer-simulated for high-mobility Si/SiGe heterojunction CMOS transistors. Comparing 0.2 $\mu$m Si/SiGe FETs to bulk Si FETs, an increase is predicted in current drive of 125% and 23% in the p-FET and n-FET, respectively. For given propagation delay (55 ns), simulated loaded ring oscillators at 1.5 V exhibit 4.6 times reduction in power-delay-product compared to bulk Si CMOS oscillators of same design rules operating at 2.5 V.

### Introduction

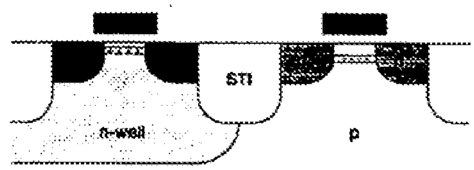
The use of strained Si/SiGe quantum wells promises to improve the performance of silicon MOSFETs by offering higher electron and hole mobilities (1,2). Si/SiGe p-MOSFETs have been fabricated by various groups (3-5). Welser, et. al. (6) have discussed the possibility of combining surface- or buried-channel NMOS with, correspondingly, buried- or surface-channel PMOS in Si/SiGe in order to achieve CMOS action.

We propose a design for Si/SiGe heterojunction CMOS (HCMOS) which, unlike previous proposals, is planar and avoids inversion of the parasitic surface channel within the designed operating voltage range. We present results of simulations which demonstrate the feasibility of this design. The performance leverage of high-mobility devices over equivalent bulk silicon NMOS and PMOS at 0.2 $\mu$m effective channel length is predicted by 2-D hydrodynamic simulation. The suitability of a high-mobility CMOS for low-power applications is demonstrated using dynamic simulations of ring oscillators.

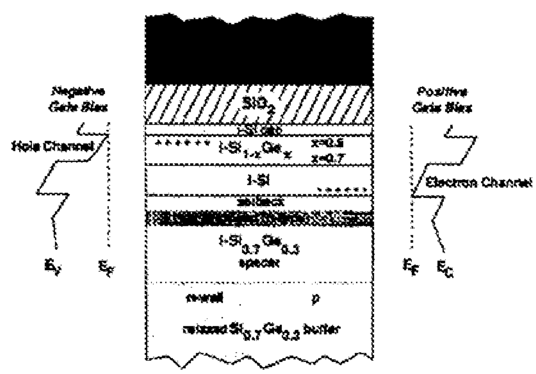
### Layer Design

Fig. 1 shows a schematic cross section of the proposed layer structure. The design provides for both a compressively-strained SiGe hole channel and a tensely-strained Si electron channel in a single planar structure. The layers are grown upon a low-defect-density ($1 \times 10^5$ cm$^{-2}$) relaxed SiGe buffer achieved using a graded buffer technique (7). The p-well is in-situ doped during growth of the relaxed buffer, while the n-well is created by ion implantation prior to growth of the channel layers. An undoped spacer is grown above the well doping in order to adjust the threshold voltage.

As shown in Fig. 1(b), an n-type $\delta$-doped layer is used to bend the energy bands so as to avoid inversion of the low-mobility silicon surface channel. The strained Si electron channel is separated from the $\delta$-doped layer by an undoped setback to minimize ionized impurity scattering. A graded Ge content is utilized in the strained $Si_{1-x}Ge_x$ hole channel in order to minimize surface roughness scattering




(a)




(b)

Fig. 1: (a) Cross section of proposed Si/SiGe HCMOS technology. (b) Schematic close-up of channel layers and conduction band and valence band for gate bias just above $V_T$. For more accurate band structure, see Fig. 4. The i- notation indicates intrinsic and undoped.

*Research Staff Member Emeritus



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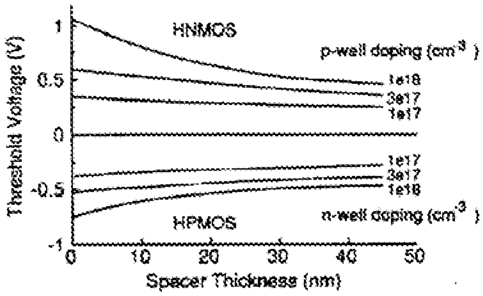


Fig. 2: Analytical calculation of HNMOS and HPMOS $V_T$ as a function of well doping and undoped spacer thickness.

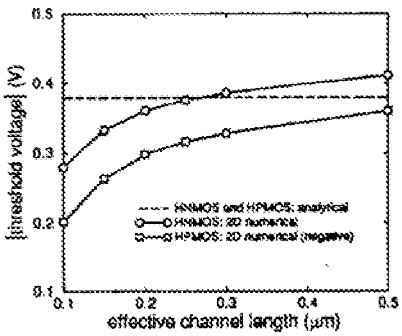


Fig. 3: 2-D numerical calculation of $V_T$ vs. channel length at $V_{DS} = 50$ mV. Shown for comparison is the long-channel value predicted by a 1-D analytical model.

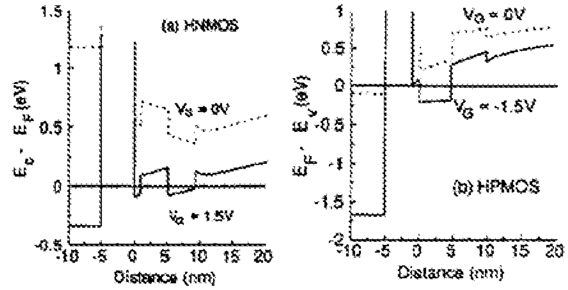


Fig. 4: (a) Conduction band under zero and 1.5 V gate bias for HNMOS. (b) Valence band under zero and -1.5 V gate bias for HPMOS.

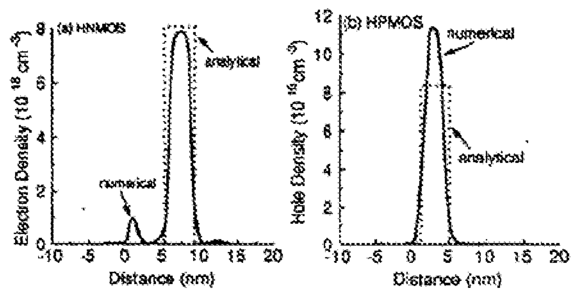


Fig. 5: (a) Electron density under 1.5 V gate bias as a function of distance from the $SiO_2$/Si interface. (b) Hole density under -1.5 V gate bias as a function of distance from the $SiO_2$/Si interface.

by shifting carriers downwards, away from the oxide. The Si cap layer allows for growth of a high quality gate oxide. An in-situ doped $p^+$ poly-Si gate is used for both devices. Different from bulk Si technology, strained Si/SiGe layers cannot be subjected to prolonged high temperature processing ($T > 800$ °C) to prevent strain relaxation and Ge diffusion. As shown in Fig. 1(a), the devices can be isolated by shallow trench isolation.

Near symmetrical NMOS/PMOS $V_T$ can be achieved with the proposed structure. Fig. 2 shows $V_T$ as a function of well doping and undoped spacer thickness as predicted by a 1-D analytical model (8). Oxide thickness is 5 nm. For the simulations, we have chosen a well doping of $3.0 \times 10^{17}$ cm$^{-3}$ and a spacer thickness of 30 nm for both device polarities, which yields a long channel $|V_T|$ of around 0.4 V. Fig. 3 shows $|V_T|$ as a function of channel length for this well doping as calculated by a 2-D device simulator.

Fig. 4 shows energy band diagrams of n- and p-channel devices under positive (1.5 V), zero, and negative (-1.5 V) gate bias as computed by a self-consistent quantum mechanical calculation. Both devices operate in enhancement mode as required. Fig. 5 shows the electron and hole distributions under positive and negative bias, respectively, comparing an analytical model to a quantum mechanical calculation. The analytical model is a first order approximation to the charge distribution, representing it as an average value within the quantum well. The model does not consider carrier population of the Si cap layer. The quantum mechanical calculation, on the other hand, shows the more accurate distributions and points out the formation of a parasitic surface channel at high gate bias. As shown in Fig. 6, however, the integrated charge density in that parasitic channel is more than an order of magnitude less than in the Si channel within the designed operating bias range ($|V_{GS}| < 1.5$ V).

### Transport Modeling

Figs. 7 and 8 show $I_D$-$V_{DS}$ and $I_D$-$V_{GS}$ characteristics, respectively, of $L_{eff} = 0.2$ μm, $t_{ox} = 5$ nm Si/SiGe HNMOS and HPMOS devices as calculated with MEDICI (9) using drift/diffusion (D/D) and hydrodynamic solutions. Also shown for comparison in Fig. 7 are simulated characteristics of bulk NMOS and PMOS devices having the same geometry and threshold voltage as their Si/SiGe counterparts. A conservative series resistance was assumed: 600 Ω μm for HNMOS and bulk NMOS, and 1800 Ω μm for HPMOS and bulk PMOS. The Si cap layer was treated

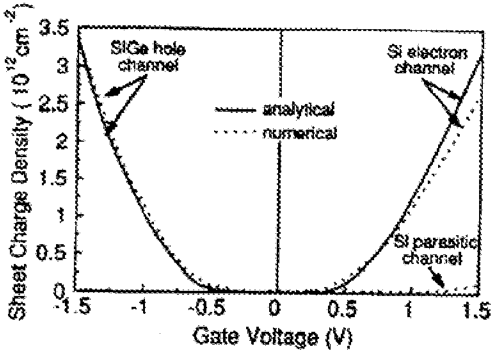

Fig. 6: Integrated charge density as a function of gate voltage.

as an insulator with the same $\epsilon$ as in Si.

The high-mobility Si/SiGe devices exhibit an increase in current drive as compared to the bulk Si devices: 23% for the n-FET and 125% for the p-FET at $|V_{GS}| = 1.5$ V. In addition, the Si/SiGe devices saturate at low drain bias: HNMOS at 0.4 V and HPMOS at 0.8 V. Extrinsic transconductances of the HNMOS and HPMOS are 441 and 288 mS/mm, respectively, at $|V_{DS}| = |V_{GS}| = 1.5$ V, an increase of 27% and 122% over bulk NMOS and PMOS, respectively, with same oxide thickness, channel length and series resistance.

In order to make a realistic comparison between Si/SiGe and bulk, low-field mobilities and transverse and parallel field dependence of mobilities were calibrated to available data. The simulation assumed low-field mobilities of 2500 and 800 cm$^2$/Vs for SiGe HNMOS and HPMOS, respectively, based on measured results in layers of similar design (2,3). The surface mobility of bulk devices followed a universal-curve dependence on perpendicular field, which, along with the parallel field dependence, was calibrated to experimental data from bulk MOSFETs (10). In the case of Si/SiGe devices, mobility was taken to be independent of perpendicular field, with the justification that the carriers are confined in a quantum well away from the oxide/silicon interface and the attendant surface roughness scattering. In the drift/diffusion solution, the same velocity saturation model was used for Si/SiGe devices as for bulk; the same value for saturated velocity was used for Si and SiGe materials ($10^7$ cm/s for both electrons and holes). In the hydrodynamic solution, the carrier temperature dependence of mobility was derived from the drift/diffusion velocity saturation model, so that the two solution types coincided in the limit of uniform electric field.

Fig. 9 shows effective carrier velocity ($g_m/WC_{ox}$, where $g_m$ is the extrinsic transconductance, W is the gate width, and $C_{ox}$ represents the effective capacitance per unit area

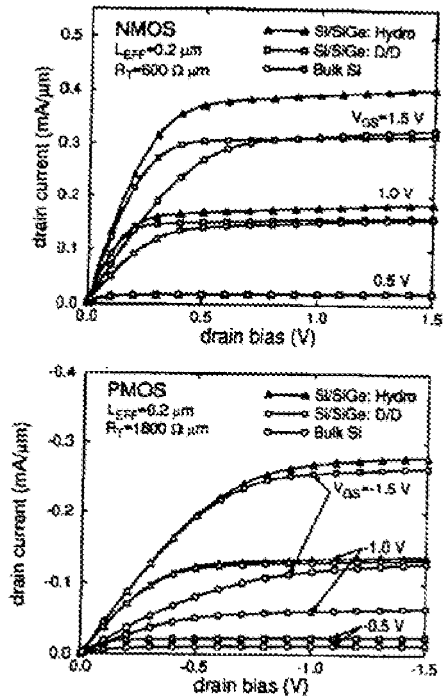

Fig. 7: Drain current vs. drain bias at three gate bias values: HNMOS (a) and HPMOS (b) vs. bulk Si. Also shown is the comparison between the drift-diffusion and the hydrodynamic calculation for HNMOS and HPMOS.

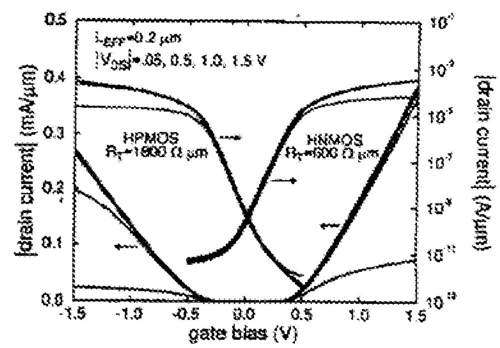

Fig. 8: Drain current vs. gate bias characteristics of HNMOS and HPMOS at four different values of drain bias.

between the gate polysilicon and the buried channel) plotted as a function of drain-induced barrier lowering, or DIBL ($\partial V_T/\partial V_{DS}$). For comparison, several state-of-the-art bulk NMOS technologies are shown. Lower series resistances of 300 and 900 $\Omega\,\mu$m for HNMOS and HPMOS, respectively, were assumed in generating this figure only. The higher electron mobility in the HNMOS results in higher effective carrier velocity than achievable in bulk

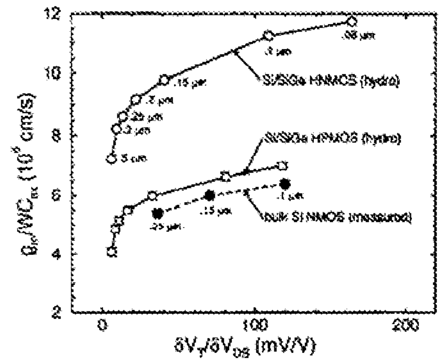


Fig. 9: Effective carrier velocity ($g_m/WC_{ox}$) as a function of DIBL ($\partial V_T/\partial V_{DS}$). The data points are labeled with effective channel lengths. The HPMOS points have effective lengths corresponding to the HNMOS points.

NMOS. Velocity overshoot is predicted to occur for channel lengths less than 0.15 $\mu m$. Note that the HPMOS curve matches the performance of bulk NMOS.

## Circuit Modeling

Fig. 10 shows the power-delay-product vs. stage delay of a simulated 11-stage inverter ring oscillator, comparing $L_{eff}$ = 0.2 $\mu m$ Si/SiGe HCMOS to bulk Si CMOS for unloaded and loaded ($C_L$ = 10 fF) cases. The HSPICE (Meta-Software) program was used with level 28 (modified BSIM) MOSFET models which were fitted to our simulated data. In the unloaded case, minimum size devices ($W_p = W_n = 1.0$ $\mu m$) were used, while in the loaded case, a ratio of 2.5:1 $W_p$:$W_n$ was used. The fan-in and fan-out were both one.

The high carrier mobility of the HCMOS results in a 6.4

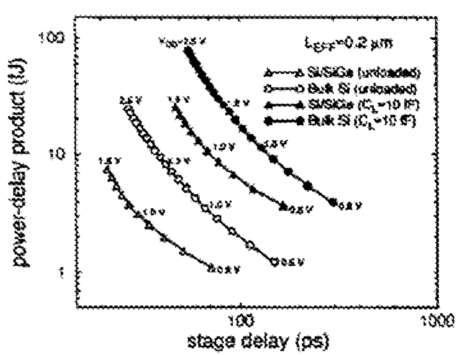


Fig. 10: Power-delay-product vs. stage delay for Si/SiGe HCMOS and bulk Si CMOS. The corresponding drain bias values are indicated on the curves.

times improvement in power-delay-product at a stage delay of 28 ps for the unloaded case, and a 4.6 times improvement at a delay of 55 ps for the loaded case. A minimum delay is demonstrated of 22 ps for the unloaded Si/SiGe HCMOS running at 1.5 V. Note that this performance cannot be matched by bulk Si CMOS of the same channel length within its breakdown limits.

The circuit performance advantage results largely from the increased current drive of the Si/SiGe p-FET, though the n-FET also contributes. In addition, since much of the switching cycle occurs in the linear regime, the earlier saturation of the drain current with drain voltage of the high-mobility devices contributes to the faster switching speed.

## Conclusion

A planar design is proposed for high-mobility SiGe heterojunction CMOS technology. Device and circuit simulations show the performance leverage of this technology over bulk Si CMOS for $L_{eff}$ = 0.2 $\mu m$. The simulations also address the general issue of the importance of mobility in sub-micron device performance (11), showing how the benefits of increased mobility persist at $L_{eff}$ = 0.2 $\mu m$ despite the onset of velocity saturation.

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